# TRENDS IN DEVICE SEE SUSCEPTIBILITY FROM HEAVY IONS

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*Abstract*

A sixth set of heavy ion single event effects (SEE) test data have been collected since the last IEEE publications (1, 2, 3, 4) in December issues of IEEE - Nuclear Science Transactions for 1985, 1987, 1989, 1991 and the IEEE Workshop Record, 1993 (5). Trends in SEE susceptibility (including soft errors and latchup) for state-of-the-art parts are evaluated.

*Introduction*

Ongoing SEE test programs at JPL, The Aerospace Corporation, the European Space Agency (ESA), CNES and other organizations are continuing; to assess specific part performance for interplanetary and satellite environments and to establish SEE response trends of an ever-increasing body of devices.

In 1985, Nichols et al (Ref. 1) published the first nearly comprehensive listing of SEE test data for 186 parts. This presentation was updated in 1987 (Ref. 2) with the publication of data for 83 additional parts, in 1989 (Ref. 3) with data for 154 parts, in 1991 (Ref. 4) with data for 182 parts, and in 1993 (Ref. 5) with data for 165 parts. In this paper, the authors extend the data base for 284 new parts. As before, the data are collected according to technology, function and manufacturer in order to identify trends, generalizations and data gaps.

*Testing Approaches*

The experimental procedures, such as those used by JPL and The Aerospace Corporation, are evolutionary and are described in detail from time to time in December issues of IEEE Transactions on Nuclear Science (6,7) or in in-house reports. In general, procedures comply with the guidelines for SEE testing set forth by the ASTM E1.11 document (8). They also comply with a JEDEC 13.4 document presently in preparation (9).

*Organization and Scope of Data*

This paper summarizes soft error and latchup experimental test data from the Jet Propulsion Laboratory (JPL), The Aerospace Corporation (A), the Goddard Space Flight Center (GDD), John Hopkins Applied Physics Laboratory (JH), Centre National D'Etudes Spatiales (CNES, France), European Space Agency (ESA), Lawrence Livermore National Laboratory (LLNL) and other SEE testers. These data are provided directly to JPL or were otherwise made available to the community during the two-year period from January, 1993, through December, 1994. We are pleased to include smaller SEE data sets generated by all U. S. and foreign researchers when these data are made

directly available to us. Not included are data sets on power transistor SEE obtained by JPL, Rockwell, Boeing and others anti published by Nichols et al (10) in 1994.

The SEE data presented here and in the previous five reports (1,2,3,4,5) represent a substantial majority of all test data obtained on SEE throughout the world. Some additional data may exist in other articles of this conference's IEEE Workshop Record or Transactions, in other journals or in published and unpublished presentations of SEE symposia.

The data from all organizations are summarized and collected together even though there may be some differences in the data from each organization. For example, JPL defines the threshold LET as that value of LET where soft errors are first counted at fluences of $10^6$ ions/cm$^2$; Aerospace now defines their LET threshold as occurring at that point where 10% measured upset cross section is 0.01 times the measured maximum cross section, CNES reports a threshold at 0.1 times the saturated cross section. JPL's definition virtually guarantees no upset below threshold but results in an overestimate of error rate if the cross section is erroneously assumed to be constant at all LETs greater than the threshold LET. Specifying a threshold LET at a fraction of the saturated cross section attempts to approximate the error rate better, but it introduces an arbitrary factor (to account for the slope of the cross section vs. LET) and an assumption that the saturated value is known and/or achieved with the highest LET ions.

The best way to calculate error rates is to use the full curve of cross section vs. LET, which may be available from the parent test organization, and integrate it over all angles and all ions of various LETs. But even this method, which involves the use of a computer, relies critically on what assumptions are made about grazing ion impacts and the dimensions of the device cell's sensitive volume.

All data are now presented here in one table, for the first time. All data listed here represent a substantial abbreviation and ignore statistical features altogether. LET limits are for nominal effective values without correction for degradation that can occur when an ion traverses device overlayers. Gold data, in particular, are seldom as damaging as one would expect on the basis of nominal LET and such data are labeled when known. SEE tests use a dynamic nominal bias (often 4.5 or 5.0 V); latchup tests are usually performed at the maximum value of the nominal bias range (e.g. 5.5V) -- a condition usually (but not always) enhancing the possibility of latchup. Reported data were taken at room temperature or ambient temperature; higher test temperature measurements do exist for some parts. In particular, latchup is known to occur more readily at higher temperatures. In some instances, data on transients is noted, which may or may not impact electronics down the line. Cross sections for transients are strongly dependent on what voltage (or current) is taken as the definition of a countable transient. Hence, a system designer interested in a specific part is again urged to contact the appropriate test organization for further information.

Users are cautioned that manufacturers (Appendix I defines manufacturer abbreviations) may often change their process, and resultant SEE susceptibility, without changing the part number or notifying tester organizations. Hence, a test of flight parts is always a good policy.

*Trends & Limitations*

Trends and device comparisons in the recent data are offered in the "Remarks" column of Tables 1 and in the following section. However, the organized tabular format is designed to facilitate comparisons. Special studies (such as variation of SEE response with temperature) or a comparison between high energy (GANIL) heavy ion data and that from the lower energy Berkeley 88-

inch cyclotron and BNL Van de Graaff are beyond the scope of this presentation.

Some colleagues have commented that a measure of the shape of the cross sections vs. LET might be useful -- such as given by a tabulation of the Weibull parameters. Others point out that it may be more difficult to assure that such parameters are properly derived and applied than it is to calculate SEE rates directly from known (and readily available) experimental cross sections.

Program managers concerned with critical system reliability issues will ultimately need an appropriate set of cross sectional data to assess statistical features and focus on specific answers. Ballpark estimates will also have a place, however, by helping assure that expensive experiments are limited to only critical SEE issues.

*An Evaluation of SEE Data*

All data are broken down according to certain functional categories for ease of reference and convenience in comparison. The data in Table 1 can be broadly grouped as microprocessors/microcontrollers, logic devices, FIFO's, all classes of RAMS, ROMs, ASICs, gate arrays, A/D and D/A converters, miscellaneous devices, DC/DC power converters (for the first time), and a widely expanded group of linear devices. In a few instances a given device may belong to more than one category but will usually be listed in only one. Hence someone seeking a specific device should try several categories if necessary.

Following are some highlights of each of these categories.

Microprocessors & Microcontrollers

JPL, 11 NL and others have obtained a large body of SEE data for microprocessors this year, all with 32-bit and (in one case) 64-bit capability (DEC's Alpha.) Soft error thresholds are consistently low for most of these high-capability machines, with LET (th) ranging from approximately 1 to 10 MeV/(mg/cm$^2$). An important exception is the Mongoose (R3000) RISC microprocessor -- a rad hard version of the R3000 based "Cobra". Most of these microprocessors were also very susceptible to latch up, although the Mongoose and the TMS 680020 microprocessor (based on SOI technology) were outstanding exceptions.

Kimbrough (11) obtained data for all commercial manufacturers' 32-bit RISC microprocessor that are presented in this year's compilation. He compared his data vs. similar data reported earlier by ESA (12), on the basis of different test approaches. He notes also that registers and functional blocks using register architecture dominate the SEE cross section. It is interesting to note that the R3000A, which is a 60% "physical" shrink of the R3000, exhibits a ~3 times larger cross section -- showing that physical device size is not, by itself, a useful figure of merit.

Testing of microcontrollers and various other processors included 8-bit, 16-bit and 32-bit machines. All of these devices were very susceptible to soft errors arnd latchup with the single exception of one device (87C51) manufactured with UTMC's rad hard design from a CMOS/bulk application specific IC [ASIC]. Some SPARC chips were tested during this period, under the aegis of Estreme (13) and Beaucour (14).

Questions regarding the best approach to microprocessor testing remain open. Some argue that static testing of known registers in a known state is the best approach to understanding SEE effects. JPL presently pursues this view and has demonstrated that not all elements of a microprocessor are equally SEE-susceptible. Others claim that testing with dynamic programs (the more the better) will usually show that static tests provide an unrealistic worst case. Dave Myers has been preparing a document describing good practice for microprocessor testing for the AS-IM (15).

'1 he European groups in this category are represented by Dr. J. Beaucour of Matra Espace who took test data at GANIL, the higher-energy (10 to 100 MeV/amu) cyclotron in France. His results provide no basis for comparison with the lower energy ions commonly used at Brookhaven's (BNL) Van de Graaff and the UC Berkeley 88-inch cyclotron. However, Dr. Beaucour (16) observes that he sees no significant difference between data he has obtained on many occasions at both BNL anti GANIL.

Logic Devices

'1 he era of broad scale testing of logic devices may be over, for only a few devices were tested. One low power device using IDT 's CEMOS technology (3,3 V/5V) was tested, showing latchup at LET = 25 MeV/(mg/cm$^2$). The response of a Harris H CMOS and NSC F ACT device were Consistent with previous data for these technologies; they exhibited no susceptibility to latchup.

J-IF(YS

Several f IF O's were tes ed. All exhibited latchup at low LET, One test of IDT devices with four diff erent epi thicknesses showed, as expected, that thinner epi devices are less susceptible to latchup.

Static RAMs (SRAMs)

Several dozen SRAMs by fourteen different manufacturers, ranging mostly from 64 kbits to 1 Mbits, were tested in this two-year period. All were varieties of CMOS technology, and almost all were very susceptible to soft errors, with LE '1 thresholds of <1 to ~5 MeV/(mg/cm$^2$). At suet-r low 1 E '1 s, one can expect proton-induced soft errors. When proton data has also been taken, that fact is noted. Most SRAMs were resistant to latchup, but some bulk CMOS technologies were very latchup-prone. The notation involving ">" or "<" signs indicates a threshold that was not obtained because of an upper or lower limit on the LE 1 of the test ion. Multiple errors per ion strike, multiple errors per single word, and perma nent hard errors were all observed in some devices. '1 here are also now extensive investigations of hard errors in SHAMS, D RAMs and FPGA's pointing to failures arising from localized total dose deposition or heavy-ion-induced rupture of individual cell oxide layers at high densities.

A few SF {AMs that were "hard" to troth soft errors and latchup were developed by IBM, Honeywell and United 1 echn ology Micro Center. Whether any of these development parts have evolved into a commercial part can be learned from the manufacturer.

Dynamic RAMS (DRAMs)

D RAMs of seven manufacturers, almost all 4M to 16M CMOS technologies, were tested this period. None exhibited latchup with the exception of the MCN MT4CM4B1DW 4Mx4 CMOS DRAM tested by Goddard SF C. All were extremely susceptible to soft errors, however, with 1 ET thresholds often extending below 1 MeV/(mg/cm$^2$) and with very thigh cross sections of the order of 1 cm$^2$ per device. Some devices exhibit functional loss at mid-range LETs of 12 to 25 MeV/(mg/cm$^2$) and also stuck bits. Some exhibit row and column errors that are not controlled by Error Correction Codes (ECC). However, ECC generally offers a dramatic improvement ir-r susceptibility, consistent with the expectation that it will be extremely unlikely for two upsets in the same word to occur at the same time. [Note that two or more physically adjacent upsets are not likely to be in the same word's electronic configuration.]

## Programmable Read Only Memories (PROMs)

A fusible-link PROM, a bipolar PROM, a UVEPROM and fifteen electrically erasable CMOS EEPROMs were tested this period. No generalizations are warranted for the individual PROM types, and norm appear fot the EEPROMs either. However, note that several of the EEPROMs are prone to latchup, anti several are not, so device selection on this basis is worthwhile indeed. Clearly, the! bulk CMOS variations of Seeq technology are not acceptable for t-nest radiation environments. Note also that several tested devices exhibit stuck bits or hard errors. In addition, a special test by JPL [submitted as a late news letter to this conference] showed that one device type, when operated in the "idle" mode, was susceptible to an "accidental write", a complete 8-bit byte write of "all 1 's", 'The Idle mode is part of the normal Read cycle! and is activated by energetic heavy ions when the device is selected and the outputs are disabled. JPL's work supplements an earlier report of Bradley et al. [Ii']. In addition, John Hopkins Applied Physics Laboratory observed a byte write it-r April, 1990 , but that detail was omitted in the compendium entry in Ref. 4 for the SEQ 28C256 EEPROM. One can now ask what device parameters or processes determine which other EEPROMs arc subject to these accidental writes in the Idle mode.

Almost all devices had very low 1 E 1 thresholds for soft errors, usually lower in the worse case "write" mode. One or two devices appear to be much harder than the rest, according to preliminary or partial test data. More test effort is required to prove this out.

## Application Specific IC's (ASIC's) & Gate Arrays (GA)

No ASICs arc! listed separately in 'Table 1 for this period. However, a few ASICs are listed under their programmed function instead. Previous data show that ASIC SEE performance varies widely, as" does their fabrication process.

Several gate! array types were tested, however; especially field programmable gate arrays (FPGA's). 'The FPGA's from several manufacturers are rather hard, with medium or high soft error LET thresholds and no propensity for latchup. Actel devices, including several process variations, all use an ONO (oxide-nitride-oxide) "antifuse" programming technology. They have been extensively tested by Aerospace and John Hopkins Applied Physics Laboratory.

In addition, JPL has tested Actel devices with high LET ions (Au and 1) and found that ions with 1. E 1>43 MeV/(mg/cm$^2$) can program antifuse connections that are initially unprogrammed when the device is operated with the normal supply voltage (5 V). JPL's A. Johnston & G. Swift (18) have postulated that these permanent failure modes may arise from single event dielectric rupture (SEDR) of the antifuse. The threat probability for present day devices is extremely small, but attempts to harden devices may greatly exacerbate the problem in the future. Manufacturers arc! currently working on devices with thinner dielectrics and lower programming Voltage requirements, which may be more sensitive to this effect. Smaller scaling is also likely to increase the problem.

## Programmable Logic Arrays and Devices (PLA's & PLD's)

Several PLA's and PLD's were! tested this period. All had fairly low soft error thresholds around an 1 ET of 7 to 10 MeV/(mg/cm$^2$). The bipolar PLA's anti the Atmel CMOS PLA were resistant to latchup, but the CMOS PLD's all latched up. These data serve to reinforce the reality that CMOS devices are likely to latch up unless special hardening processes are used. In the latter event, their latchup susceptibility is less, but not always zero. It is a fact of life that the inclusion of an epi layer does not provide an

iron clad guarantee against latchup, because the epi thickness may be too great for the particular device. Exactly how thin the epi thickness must be cannot be answered by an experimental data base; it depends on the intrinsic susceptibility of the device in question.

Linear Devices

1 inear devices have received much more attention recently, mainly from GSFC anti Aerospace. I-his arises from the recognition that heavy-ion-induced transients may cause a problem in adjacent circuitry even though there are no latches or bistable states in the test devices themselves. '1 he data in Table 1 for linear devices is listed under category 18, which is broken down further according to function.

(1) 7 ransceiver and 1 ransmitter-Receiver pairs: T here! is much GDD (GSFC) data for several manufacturers. Gazelle?'s two GaAs devices show no latchup nor do **the** bipolar silicon devices [All devices are silicon unless otherwise stated. ] However, CMOS and IDT's new low power CE M(IS technologies are susceptible to latchup. There is also a soft error tabulation of LET thresholds, but the "<" sign indicates that the ion LET was not low enough to establish the device threshold LET for many of the test runs. A fuller interpretation of these data are given in the **listed** reference (19).

(2) Op Amps: T here are no latchups reported for the bipolar op amps, with one exception as noted under "Remarks." This identification of a bipolar latchup is not generally accepted. The real concern is that op amps may exhibit transients of sufficient duration anti amplitude to upset a latch in adjacent devices. '1 est data have been obtained for fifteen op amps as shown in T able 1. The manufacturers receiving most of the SE E testing are NSC anti F'MI. A variety of op amps have rather low L ET thresholds, corresponding to a wide susceptibility to inter-galactic heavy ions. In some cases [when 1 ET< 8 MeV/(mg/cm2)], protons may cause these transients although that remains to be proved. These LET thresholds and the corresponding cross sections depend, of course, on what amplitude and/or duration are considered large enough to count as a 'damaging' transient. 1 here is at present no standard-sized transient, and this may be just as well, for there is also no standard transient that will pose a threat to any specific system under evaluation. Most transients are in the neighborhood of <1 to 20 microsec duration and have amplitudes ranging up to several volts.

A cursory look at some systems shows that transients of these durations can be dangerous. The saving grace will be that the cross section for dangerously large voltage amplitudes may correspond to a very low upset rate (<one per year) for many devices in the galactic cosmic ray (GCR) environment. 1 hese rates, which are proportional to measured transient cross sections, are very sensitive to the transient voltage amplitude, however, so one cannot safely embrace any generalizations without obtaining system information on tolerable amplitudes anti durations.

(3) Other linear devices: Much data is also available for less critical components, such as voltage regulators, comparators, switches, drivers, receivers and driver-receiver pairs.

DAC's and ADC's

There is considerable data on digital-to-analog converters (DAC's) and analog-to-digital converters (ADC's), grouped separately under category 19. There is a further subgrouping, according to the number of bits (or resolution) that the devices can process.

Most of the data for the DAC's is directed at ascertaining whether they latchup. None of the tested devices latched up. A review of earlier DAC data (Refs. 1,2,3,4,5) show that none has ever latched up, even

though some appear to be CMOS technology. In this recent period, there is one 8-bit Harris DAC that also appears to be immune to soft errors. This is such an unusual departure from DAC susceptibility to very low LET ions, that the test approach and/or fabrication process for that device might merit further investigation.

For the ADC's, data sets for both "soft error with latchup" and "latchup only" are presented. For ADC's, latchup of CMOS devices is possible, and soft error LET thresholds are consistently low. However, testing of modern ADC devices (which may comprise a RAM, latches and microcontroller) may be quite complex and the interpretation of a dynamic cross section is non-trivial (20, 21). Single event output errors can be described as either (1) Noise Errors; forming a Gaussian distribution of output values very near the nominal output, anti (2) Offset Errors; less common, but widely spaced along the range of possible digital outputs. Understanding which cross section is tabulated should be validated by the test organization; whether one or both or neither is important to a particular system's operation requires interaction between the project's designers and parts reliability SEE personnel.

One interesting line entry in I-able 1 is the reported failure of the bipolar AD I AD9048 8-bit flash ADC in which the device went into a permanent unwanted C) utput mode; most often a two's complement of the correctly converted output. This particular failure mode has been reported in Aerospace ground tests and analyzed by Koga et al (22), who present persuasive evidence that it is a distinctly different type of single event failure involving a localized second breakdown of a bipolar transistor. This type of failure was also exhibited in orbit on one of two parallel lines of the TOPEX satellite's Star Tracker system. Here the inverse operation [now disabled] would act to open the tracker shutter' wide when looking at the sun, and close it tight during normal night scanning.

DC/DC Power Converter

A new device category is opened up here, because nine DC/DC power converters were tested during this period. As seen in Table 1, a wide variety of device responses is possible. One CMOS device latched up. Also observed are many non-destructive conditions involving voltage drops, voltage spikes and reset errors. Two ADA bipolar devices displayed switchoff errors which are tentatively attributed to a gate rupture (SEGR) that switches "on" a power MOSFET embodied in the converter.

Miscellaneous Devices

Many miscellaneous devices are tabulated under the last category #/21, and some other devices from categories 16 and 17 have not been included in the text, Some devices may properly belong in one of the other categories, so take a look here if you desire a complete survey of the data. Note that a few fiber optic devices are included as well as special controllers.

*Conclusions*

The new data presented here can be combined with data given in References 1 through 5 to develop certain generalizations useful for protecting flight electronics from SEE". Hard technologies anti unacceptably soft technologies can be flagged. In some instances, specific tested parts can be taken as candidates for key functions-- such as microprocessing or memory, As always with radiation test data, specific test data for qualified flight parts is recommended for critical applications. Calculations of accurate SEE rates will require the assistance of a computer code, a w(!ll-defined environment [in terms of flux vs. LET] and a complete device characterization [cross section vs. LET at the appropriate temperature.] Finally, assessment of flares needs to be considered.

Evaluation of catastrophic effects requites its own statistical treatment. Data

for power transistor burnout and single event gate rupture is not included here; one may refer to Nichols et al, (10).

The most recent 1995 data is not her-e-- see JPL's RADATA data base (23).

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*Appendix I-- Manufacturer Abbreviations*

The following is a list of manufacturers who have appeared in all of the compendia of data, Not ail of those listed here appear in this year's data set.

| | |
|---|---|
| ACT | Actel Corp. |
| ADA | Advanced Analog |
| ADI | Analog Devices Inc. |
| AFX | Aeroflex Labs |
| ALS | Allied Signal |
| ALT | Alters Corp. |
| AME) | Advanced Microdevices Corp. |
| APX | Apex |
| ATM | Atmel |
| ATT" | American T-cl & Tel |
| BAL | Bal Efatrom |
| BUB | Burr-Brown Research |
| CPT | Crosspoint |
| CRY | Crystal Semiconductor Inc. |
| CYP | Cypress Corp. |
| DAT | Datel |
| DDC | DDC ILC Data Device Corp. |
| DEC | Digital Equipment Corp. |
| EDI | EDI Corp. |
| ELN | Elantec |
| FAS | Fairchild Semiconductor Div. |
| FER | Ferranti |
| FUJ | Fujitsu ltd. |
| GAZ | Gazelle |
| GE-C | General E lectric |
| HAR | Harris Corp., Semiconductor Div. |
| I-I-I-c | Hitachi Ltd. |
| HON | Honeywell Inc. |
| HPA | Hewlett-Packard Corp. |
| HYB | Hybrid Systems |
| IBM | IBM |
| IDT | Integrated Device Technologies, Inc. |
| INM | INMOS Corporation |
| IN-[ | Intel Corp. |
| ISM | INMOS Corp. |
| ITP | Interpoint |
| LDI | Logic Devices Inc. |
| L1N | Linear 1 echnology |
| LSI | LSI Logic Corp. |
| MCN | Micron Technologies |
| MDI | Modular Devices, Inc. |
| MED | Marconi E lectronic Devices |
| MIC | Micrel Semiconductors |
| MIR | Micro-Rel Corp. |
| MIT | Mitsubishi |
| MMI | Monolithic Memories Inc. |
| MOC | Mosaic Semiconductor |
| MOT | Motorola Semiconductor Products Inc. |
| MPS | Micro Power System |
| MT"A | Matra Harris Semiconductor |
| MXM | MAXIM |
| NCR | National Cash Register |
| NEC | Nippon E. lectric Corp. |
| NSC | National Semiconductor Corp. |
| NTL | Natel Engineering |
| OKI | Oki Semiconductor, Inc. |
| o w I | Omni-Wave!, Inc. |
| PFS | Performance Semiconductor Inc. |
| PLS | Plessey Semiconductors |
| PMI | Precision Monolithic, Inc. |
| RAY | Raytheon Co., Semiconductor Division |
| RCA | Radio Corporation of America |
| RMT | Ramtrcm |
| SAM | Samsung |
| SEI | Seiko |

SEQ SEEQ Technology Inc.
SGN Signetics Corp.
SGP Signal Processing
SIE Siemens Components, Inc.
SIL Siliconix
SIP Sipex
SLG Silicon General
SNL Sandia National Laboratories
SNY Sony Corp.
SOR SOREP
SSD Solid State Devices
STC Silicon Transistor Corp.
TEL Teledyne Crystalonics
TIX Texas Instruments Inc.
TMS Thomson Military & Space, France
TOS Toshiba
TRW TRW Inc.
UTM United Technologies Microelectronics Center
WAF Waferscale
WDC Western Digital Corp.
WEC Westinghouse Electric Corp.
XIC Xicor Inc.
XIL Xilinx Corp.
ZOR Zoran
ZYR Zyrel

*Appendix II-- Test Organizations*

A The Aerospace Corporation; El Segundo, CA
ADI Analog Devices Semiconductor, Wilmington, MA
ALC Alcatel Espace, Toulouse, France
Ball Ball Aerospace Systems Division, Boulder, CO
BDS Boeing Defense & Space Group, Seattle
BPS Boeing Physical Sciences Research Center, Seattle
CERT 2, Avenue Edouard Belin, Toulouse, France
CLM Clemson University; Clemson, SC
CNES Centre National d'Etudes Spatiales; Toulouse, France
DASA Deutsche Aerospace AG, Munich
ESA European Space Agency -- several facilities
GD General Dynamics
GDD NASA Goddard Space Flight Center; Greenbelt, MD
GE GETSCO, Philadelphia
HAR Harris Semiconductor
HAC Hughes Aircraft
HON Honeywell
IBM IBM (See Remarks column).
J Jet Propulsion Laboratory (JPL); Pasadena, CA
JH John Hopkins Applied Physics Laboratory; Laurel, MD
LIN Lincoln Laboratories, M. I. T.; Cambridge, MA
Loral Loral, Manassas, VA
LLNL Lawrence Livermore National Laboratory; Liverrnore, CA
MM Martin Marietta Astrospace, Valley Force, PA
MMS Matra Marconi Space; Vélizy, France
MOT Motorola GSIG
NASA National Aeronautics & Space Administration
NRL Naval Research Laboratories, Washington D. C.
NWSC Naval Weapon Support Center, Crane, IN
PHY Physitron , Inc., San Diego
R Rockwell international, Anaheim, CA
SNL Sandia National Laboratory, Albuquerque
Soreq, Isr. See Remarks Column.
SSS S-Cubed, San Diego
TRW TRW Space and Defense Sector; Los Angeles
UTM United Technologies Microelectronics Center, Colorado Springs

*Appendix III-- Test Facilities*

88-in. = 88-inch cyclotron, Lawrence Berkeley Laboratory, Berkeley, California

BNL: Tandem Van de Graaff, Brookhaven National Laboratory, Long Island, NY

Cf-252 = A Cf-252 fission source. The data from this type of source is rarely given because of inaccuracies inherent to the limited range of the fission ions.

ESA: European Space Agency -- several sites

GANIL= Cyclotron for High Energy Heavy ions; Caen, France

GSI= Cyclotron for High Energy Heavy Ions; Darmstadt, Germany

HAR= Van de Graaff at Harwell, England

IPN= Tandem Van de Graaff, Institut de Physique Nucleaire; Orsay, France

UW= Tandem Van de Graaff, University of Washington , Seattle

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For support, call Sam Farmanesh:
Voice: (81 8)354-1 968
FAX: (81 8)393-4559
e-mail: farmanesh@jpl.nasa.gov

Table 1. SEU Data

| | Test Org * | Device | Function | Technology | Mfr | Bits | Effective LET** Threshold | Device Cross Section (cm2)*** | Cross Section Per Bit (sq mic) | Facility **** | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | 34304 | | |
| | Test Org * | Device | Function | Technology | Mfr. | Bits | Effective LET** Threshold | Device Cross Section (cm2)*** | Cross Section Per Bit (sq mic) | Facility | Remarks |
| 2 | A | 80C286 | MicroP (16-bit) | CMOS | HAR | — | 12 | 1E-3 | — | | No LU>90 Koga ~94 Private Comm Compare earlier CMOS/epi data |
| 3 | MMS | 7C601 | MicroP (32-bit) SPARC | CMOS bulk 0.8 mic | CYP | — | — | — | — | GANIL | LU(th)=10; 1.8E-2 cm2 Beaucour, 93! EEE-NS Workshop |
| 3 | LLNL | R3000A | MicroP (32-bit) RISC | CMOS 6-- 0.8 mic. | IDT | See ref | ~5 | 1E-3 | — | 88-in | LU=14 to 24; 2E-4cm2 J Kimbrough, IEEE NS, Part II, p 2706 (Dec 94) |
| 3 | HAC | 80960MX | MicroP (32-bit) | CMOS | INT | — | — | — | — | 88-in | LU(th)=15; 1E-3 cm2 Two LU modes 30 & 100's of mA Shoga 3/93 |
| 3 | CNES | L64811 | MicroP (32-bit) SPARC | CMOS | LSI | Reg & application | 2 | 2E-3(reg only) | — | IPN | LU(th) -A. = SE-2 cm2 Estreme et al, IEEE93 Registers , applications |
| 3 | MMS | L64730 | DCT processor | CMOS | LSI | — | — | — | — | GANIL | LU(th)=8;2E-3Beaucour, 93!IEEE Workshop |
| 3 | GDD | Mongoose (R3000) | MicroP (32-bit) RISC | HCMOS (1.0 mic.) on epi | LSI | Core, reg, ALU | 23 | >3E-6 (Sat= 4E-5) | N/A | BNL | LU(th) >85 LaBel 94!EEE Workshop A RH version of R3000-based "Cobra" |
| 3 | LLNL | R3000A | MicroP (32-bit) RISC | CMOS-- 0.7 mic | LSI | See ref. | <2.8 | 2E-3 | — | 88-in | LU(th)= 38 1062,2.55 cm2 J Kimbrough, IEEE-NS, Part II, p 2706 (Dec 94) |
| 3 | LLNL | R3000HC | MicroP (32-bit) RISC | CMOS-- 1.0 mic. | LSI | See ref | 3 | 5E-3 | — | 88-in | LU(th)= 24 to 38; 1.E-3cm2 J Kimbrough, IEEE-NS, Part II, p 2706 (Dec 94) |
| 3 | CNES | 90C601 SPARC60* | MicroP (32-bit) SPARC | CMOS/bulk | MTA | Varies | 2 | 8E-3 (reg only) | — | IPN & Cf-252 | LU(th) <13; = 2E-3 cm2 Estreme et al, IEEE93 Registers , applications |
| 3 | LLNL | R3000A | MicroP (32-bit) RISC | CMOS | NEC | See ref. | 3 | 1E-3 | — | 88-in | LU(th)= 38!053.6 E-4 cm2 J Kimbrough, IEEE NS, Part II, p 2706 (Dec 94) |
| 3 | LLNL | R3000A | MicroP (32-bit) RISC | CMOS PACE III--0.6 mic | PES | See ref | <3 | 2E-3 | — | 88-in | No LU>63 J Kimbrough, IEEE-NS, Part II, p 2706 (Dec 94) |
| 3 | LLNL | PR3400 | MicroP (32-bit) RISC | CMOS PACE III--0.6 mic | PES | See ref. | <3 | 1E-3 | — | 88-in | LU(th)=14 to 24; 1E-4cm2 J Kimbrough, IEEE-NS, Part II, p 2706 (Dec 94) |
| 3 | LLNL | PR3400A | MicroP (32-bit) RISC | CMOS PACE III--0.7 mic | PES | See ref. | <3 | 1E-3 | — | 88-in | LU(th) =38 to 53. 1 E-5cm2 J Kimbrough, IEEE NS. Part II, P 2706 (Dec 96) |
| 3 | LLNL | PR3400L | MicroP (32-bit) RISC | CMOS PACE III--0.6 mic | PES | See ref. | <3 | 1E-3 | — | 88-in | LU(th)=14 to 24; 1E-4cm2 J Kimbrough, IEEE-MS, Part II, p 2706 (Dec 94) |
| 3 | LLNL | R3000A | MicroP (32-bit) RISC | CMOS | SIE | See ref | 4 | 2E-3 | — | 88-in | No LU>63 J Kimbrough, IEEE-NS, Part II, p 2706 (Dec 94) |
| 3 | CNES | 68T020 | MicroP (32-bit) | CMOS-SOI-0.8 mic (MSOI4CB) | TMS | 697 register bits | 7 | 1.1E-3; 2.4E-3 @ LET=72 (Reg, cache enabled is W.C.) | | IPN | No LU >72 Lestrat et al, IEEE94-NS, o2240 |
| 4 | GDD | Alpha | MicroP (64-bit) RISC | CMOS | DEC | — | — | — | — | BNL | LU(th)<3 65>55.4 cm2 @ LET=11 LaBel IEEE93 preprint |
| 5 | A | AM85C30 | Controller | CMOS | AMD | — | — | — | — | 88-in | LU(th)=20; 1E-3 cm2. Koga ~1994 |
| 5 | A | AMAS2901 | Controller | CMOS/SOS | GEC-PLS | — | >120 | — | — | 88-in | LU >120. See 2901 bit-slices. Koga ~1994 |
| 5 | SNL | 82C527 | CAN Microcontroller(8-bit) | CHMOSIII/10 mic. epi | INT | 15 8-byte registers | 2 | 5E-4 at LET=25. Latchup obscures higher LET SEU data | | BNL | LU(th)=17; 2E-4 cm2 Saxton. No temp depend. IEEE94 Workshop |
| 5 | BDS | 87C51FB & 87C51FC | Microcontroller (8-bit) | CHMOSIII-E (256 byte RAM) | INT | 2300 bits | ~2 @ 18% sat | Special cross sections | 430 (RAM/RAM | 88 in | LU(th)=10 @ 6V; 1E-3 cm2. 8/92. See next Proton upsets. 93!EEE Workshop |
| 5 | BDS | BU80C51FC | Microcontroller (8-bit) | CMOS/epi | UTM (1) | "voting RAM" + reg | 20 | ~1E-4 | partial cross sections exist | 88 in | No LU>37. Baze, IEEE93, p 1703. (1)=Boeing redesign. Test 6/93. |
| 5 | J | 68HCS705 | MicroCont. (8-bit) | ? part of RF modem | MOT | — | — | — | — | BNL | LU(th)=7;>5E-3 cm2 @ LET=56; in standby mode Jun 93. |
| 5 | J | 87C552 (inc. 80C51) | MicroCont. (8-bit) | CMOS | SGN | — | — | — | — | BNL | LU(th)=11; 4E-3 cm2 in standard mode Jun 93. MicroC has 80C51 microP. |
| 5 | ESA | 82380 | DMA Controller(32-bit) | CHMOSIII, Jersusalem, mask B | INT | 111 registers | 11 | — | 10000 | BNL | LU(th)=15; 3E-6 (per device?). Microlatchup H. Van Looy, ESA Rept. 5/93. |
| 5 | ESA | 53C90 MARS94 Flight | SCSI Controller | CMOS | NCR | 168 bits | >15 | LU interfered with SEU test; Cf252 failed to detect LU. | | BNL & Cf 252 | LU(th) lies between 15 & 25 DC 8923P Harboe-Sorensen, RADECS93 p.490. |
| 6 | IBM | SM320E15 | DSP (16-bit) | | TIX | RAM & register | Rates given | — | — | BNL | Latchup rates given 5/93 DC 9145A WP-2 (Jim Pollack) See following |
| 6 | IBM | SMJ27C128-25 | EEPROM (16Kx8) | | TIX | EEPROM | Rates given | — | — | BNL | The data here is a subset of that preceding -- for the same chip |
| 6 | A | 320C30 | DSP (32-bit) | CMOS/epi (7 mic.) | TIX | — | 3 | 1E-4 | — | 88-in | LU(th)=10; 2E-4 cm2 Dec '92 & later? |
| 6 | J | TMS320C50 | DSP (16-bit) | CMOS | TIX | RAMs & Reg | 3 | >5E-2 (SRAM partial cross section) | | BNL | LU(th)=18; 3E-4 cm2 (unsat.) Compare to other version above. 8/94 |
| 6 | MMS | 7C602 | Coproc. (32-bit FPU) SPARC | CMOS bulk 0.8 mic. | CYP | — | — | — | — | GANIL | LU(th)=16.5;9.5E-3, Beaucour, 93!IEEE NS Workshop |
| 6 | MMS | 7C604 | Coproc. (32-bit MMU) SPAR | CMOS bulk 0.8 mic. | CYP | — | — | — | — | GANIL | LU(th)=10;5.1E-2, Beaucour, 93!IEEE-NS Workshop |
| 6 | J | L64801 | 32-bit Integer unit SPARC | "rad-hard" CMOS/epi(10 mic) | LSI | Registers | 7 | 2E-5 @ LET=15 | — | BNL | LU(th)=15; 8E-4 cm2 @ LET=60 3/94 SEE MMS data |
| 6 | J | L64804 | Floating Point Unit SPARC | "rad-hard" CMOS | LSI | FLPt | ~4 | 1.5E-4 @ LET=8.7 | — | BNL | LU(th)=8.7;1E-3 cm2 @LET=60 3/94 |
| 6 | CNES | L64814 | FP Coprocessor (32-bit) | CMOS | LSI | Reg & application | 2 | 1E-1 | — | IPN | LU curve same as SEU data, as given. Estreme et al, IEEE93 Workshop Record |
| 6 | CNES | 90C602 SPARC602 | Coproc. (32-bit) | CMOS/bulk | MTA | Varies | ~4 | 2E-3 (reg only) | — | IPN& C, 252 | LU(th)<27;2E-3 cm2. Estreme, IEEE93 Workshop Registers & application programs |
| 7 | GDD | 74FTC163374PV | 3.3V/5V 16-Bit Register | CEMOS (low power) | IDT | — | ~20 | — | — | BNL | LU=25; >5E-4 cm2 LaBel 5/94 Same LU as I LIT CEMOS transceiver (group 1B) |
| 7 | J | F100331 | D-FF | Bipolar/ECL(100K) | NSC | Triple | 10 | 1.7E-4 | — | BNL | No LU>85 Jun 93 |
| 7 | MV | F100336 | 4-Stage Counter/shift registe | Bipolar/ECL | NSC | — | 27(10kHz) | 1 E-51,9 kHZ) | — | BNL? | No LU>74 No SEU LET>74 at 1MHz DC 9127A 4/93 |
| 7 | ESA | TLC555 | Precision Timer | LinCMOS | TIX | — | — | — | | GANIL | LU between 10 & 20, 1E-4 cm2 H. Van Looy, ESA Rept -1993 |
| 7 | GDD | HS508RH | Analog MUX | HCMOS | HAR | — | 110 | — | — | BNL | No LU>1 ,0 LaBel 94 IEEE Workshop Record Tested 6/93 |
| 7 | J | 54ACTQ245 | Transceiver | FACT | NSC | — | — | — | — | BNL | No LU >120 1/94 |
| 8 | HON | CY7C429-30DM | FIFO | ? | CYP | 2Kx9 | <<4.3 | — | — | BNL | LU LET., 7 Pointer errors put FIFO in unknown state @ LET(th)=6.4 4/93 |
| 8 | GDD | 7201T | FIFO (512x9) | CMOS- various split epi | IDT | A test of SEL vs. epi thicknesses | | Only 6 mic (DC=JEG8334) has LU>80, SEU LET(th) <3.4 | | BNL | LU varies from <26 to >80 for 5,8,10 & 12 mic epi See RADATA LaBel 5/94 |
| 8 | GDD | 7203L40DB | FIFO (2Kx9) | CMOS | IDT | — | 3.4 | 5.5 E-3 | — | BNL | LU= 15 to22 DC 3BC9334BP LaBel 6/30/94 |
| 8 | GDD | 7203ERP | FIFO (2Kx9) | CMOS | IDT | — | 8 to 11.6 | obscured by SEL | — | BNL | LU= ~35 Destructive bursts @ LET=20 (due to control areas?) LaBel 11/94 |
| 8 | GDD | 7204 | FIFO (4Kx9) | CMOS | IDT | — | 8 to 11.6 | obscured by SEL | — | BNL | LU=16 LaBel 11/94 |
| 9 | J | CY7C199 | SRAM | CMOS | CYP | 32Kx8 | 1.5 | 0.3 @ LET=15 | — | BNL | LU(th)=1.0, 5E-4 cm2 Mar 94 |
| 9 | U. Siegen | HM1-65162-2 | SRAM | CMOS/epi | HAR | 2Kx8 | <3.6 | 0.1 (LET=62) | — | GSI | No LU> 9S @ very high energy Multiple bit errors J Dreute RADECS9 , p505 |
| 9 | — | HC6364 | SRAM | — | HON | 8Kx8 | <18 | — | — | | McNulty,IEEE93,p 1967 |
| 9 | J | HC6364 | SRAM | CMOS/epi | HON | 8Kx8 | 36 | 2E-2 | — | BNL | No LU>84 SEU data at higher T 3/93 Comparable HON data is SEU LET(th)=56 |
| 9 | HON | HC6856 | SRAM | RICMOS IV (R = 108K to 335K) | HON | 32Kx8 | 40 for 108K; >160 for >198K | | 10 (low R=108K) | BNL | Test for variations of R and temp. 27,,,< epi HON Rept of test of Nov 91(4/93) |

Table 1. SEU Data

| | Test Org * | Device | Function | Technology | Mfr | Bits | Effective LET** Threshold | Device Cross Section (cm2)*** | Cross Section Per Bit (sq mic) | Facility **** | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 9 | ESA | HM62256 | SRAM | CMOS | HTC | 32Kx8 | 3 | | | | No LU IEEE93 p 1498 DC8641 & 8845 SEUs IPN<BNL Proton data exist s |
| 9 | CNES | HM62256R | SRAM | CMOS | HTC | 32Kx8 | <1.7 | | 300 | IPN | No LU IEEE93 preprint DC9302 Proton data exists |
| 9 | CNES | HM62282H | SRAM | DC 9249 | HTC | 32Kx8 | 1.7 | | 40 | IPN | No LL, IEEE93 preprint DC9249 Proton data exists |
| 9 | ESA | HM6264 | SRAM | CMOS | HTC | 8Kx8 | -5 | — | 150 @ LET=13, then LU | BNL | LU(th) <13; 1E-3 cm2 IEEE, p 1498 (Dec 93) DC8431 Proton data exis's |
| 9 | ESA | HM6264A | SRAM | CMOS | HTC | 8Kx8 | -5 | — | 150 | IPN | LU(th)< 13. 1E-3 cm2 IEEE, p1498 (Dec 93) DC8901 Proton data exist's |
| 9 | MVS | MSM8128 | SRAM | | HTC | 128Kx8 | — | — | — | GAN'L | SHE (Single Hard Error) LET(th)= ~50; 1E-3cm2 Polvey, IEEE-NS, 2235 (1994) |
| 9 | MVS | HM628128 | SRAM | CMOS/epi | HTC | 128Kx8 | — | | — | GAN'L | No LU>1 10 Hard Errors Beaucour, 93IEEE Workshop |
| 9 | GDD | HM628128 | SRAM | CMOS/epi | HTC | 128Kx8 | <1.4 | 2.3 dyn, 0.2 static | Multiple bits per strike | BNL | No LU> t 10 LaBel, 94IEEE Workshop Record Tested 5/93 |
| 9 | ESA | HM628128 | SRAM | CMOS | HTC | 128Kx8 | ~3 | | 40 | IPN | No LU IEEE93 p 1 498 DC9009 Proton data exists |
| 9 | MVS | HM628128 | SRAM | CMOS/epi | HTC | 128Kx8 | — | — | — | GAN'L | No LU> 110 Hard errors Beaucour, 93IEEE Workshop |
| 9 | J/A | HM628128 | SRAM | NMOS/CMOS | HTC | 128Kx8 | 4 | 0.5 | 50 | 88-in | J LU(th)= 80 March 1990; A No LU>127 IEEE93 preprint |
| 9 | ESA | HM628512 | SRAM | CMOS | HTC | 512Kx8 | -2 | — | 60 | BNL | No LU IEEE93 p 1498 DC9235 A few stuck bits that anneal Proton data exists |
| 9 | IBM | 2568CPH | SRAM | RHCMOS(Manassas) | IBM | 32Kx8 | >100 | No upset | No upset | BNL | No LU> 100 From IBM Rept on Since Station (DMS)3/93 |
| 9 | GDD | 70V25 | SRAM | CMOS | IDT | 16 bit wide, dual | <3.46 | | 50 | BNL | No LU>80 Static & dynamic tests Multiple upsets LaBel test d 7/94 |
| 9 | A JH | IDT71256 | SRAM | NMOS/CMOS | IDT | 32Kx8 | 25 | 02 | — | 88-in & Beva'ac | LU=15; 7E-5 cm2 SMU's A Dec 1987 & RADECS93 JH tested Aug 90 |
| 9 | CNES | IDT7134 | SRAM | CMOS | IDT | 4Kx8 | <1 | | 300 | IPN | LU= ,2 7;7 E-4cm2 Ecoffet et al, IEEE93 Proton data exists Date Code ES |
| 9 | IBM | IMS1601EPI | SRAM | CMOS non rad-hard | ISM | 64Kx1 | -2 | 0.4 | includes multiple errors | 88-in | No LU>60 O'Neill, IEEE, p1 755 (10/94) using data of T Scott (IBM) |
| 9 | CERT | IN1630SL | SRAM | — | ISM | 8Kx8 | | 0.4 | double bit errors per data byte | IPN | No LU>72, Falguere ICE RT1, RADECS91 p479 |
| 9 | ESA | MARS94 Flight Part | SRAM | CMOS Process SO6A | MCN | 32Kx8 | ~1.5 | — | 5 | BNL | No LU>85 Harboe-Sorensen, RADECS93 preprint |
| 9 | CNES | MT5C1001 | SRAM | CMOS | MCN | 1Mx1 | <0.3 | 0.5 | 40 to 70 (pattern dependent) | IPN | Ecoffet et d. IEEE93 Workshop Proton data exists Date Code 91 33 |
| 9 | MVS | MT5C1008 | SRAM | | MCN | 128Kx8 | | | — | GAN'L | SHE (Single Hard Error) LET(th)=~50; , E 3cm2 Polvey, IEEE NS, 2235 (19Q41 |
| 9 | CERT | MT5C1008 | SRAM | | MCN | 128Kx8 | 0.6 | 1(worst "all 1's") | Includes multiple errors | IPN | No LU >36 Falguere RADECS91 p 479 |
| 9 | CNES | MT5C1008 | SRAM | CMOS | MCN | 128Kx8 | <1.7 | 1.8 | 25 to 150 (pattern dependent) | IPN | Ecoffet et d. IEEE93 & IEEE92 Workshop Proton data exists Date Cede 9,25 |
| 9 | CNES | MT5C1008 | SRAM | CMOS/epi LCRP(Ref 1) | MCN | 128Kx8 | <1.7; <7 @ 10% | 2E-2 | 0.29 checkered address | IPN | Engr sample-- LCRP= low current resis 'or process Ecoffet 92 & Workshop 93 |
| 9 | A | MT5C1008 | SRAM | CMOS/epi LCRP2 | MCN | 128Kx8 | 4 @ 10% sat | 2E-3 | Single-word multiple upsets[SMUs] | 88-in | No LU>100 Koga, IEEE93 Low cross section implies low current devices |
| 9 | MVS | MT5C1008C | SRAM | CMOS/bulk | MCN | | | — | | GAN'L | LU=75;4E-4cm2; hard errors Dufour IEEE92; Polvey IEEE 94 |
| 9 | CNES | MT5C1009 | SRAM | Date Code "ES" | MCN | 128Kx8 | <1.7 | | 0.01 to 1.2 (pattern dependent) | IPN | Ecoffet et al, IEEE93 Workshop Date Cede "ES" |
| 9 | J | MT5C2568 | SRAM | CMOS/epi (0.65 micron feature) | MCN | 32Kx8 | <1.4 | 0.05 & 0.4 (Remarks) | — | BNL | No LU >72 12/93 Cross section discrepancy needs resolution |
| 9 | J | MT5C2568-25 | SRAM | CMOS/epi (suffix=read/write(ns)) | MCN | 32Kx8 | <1.4 | 0.03 (worst "all 1's") | — | BNL | No LU >72 1 2/93 Same as next except for giant error clusters of version -70 |
| 9 | J | MT5C2568-70 | SRAM | CMOS/epi (suffix=read/write(ns)) | MCN | 32Kx8 | <1.4 | 0.03 (worst "all 1's") | — | BNL | No LU >72 12/93 Giant 32K error clusters at LET>26 |
| 9 | ESA | MT5C2568C | SRAM | CMOS | MCN | 32Kx8 | <1.7 | — | 150 | IPN | No LU >40 See later technology Harboe-Sorensen, RADECS93, p 490 |
| 9 | CERT | MT5C2568C | SRAM | | MCN | 32Kx8 | | 0.35 | — | IPN | No LU ,72 Falguere, RADECS91 p 479 |
| 9 | J | MSM8128K | SRAM | CMOS? | MOC | 128Kx8 | 2.8 | 4E-3 (LET=26) | — | BNL | LU(th)=26 Dec 13, 19S3 |
| 9 | J | MSM8128KL | SRAM | CMOS? | MOC | 128Kx8 | 2.8 | 4E-3 (LET=26) | — | BNL | LU(th)=26 Dec ,3, 1993 No difference between -K and -KL versions |
| 9 | ESA | MHS65162 | SRAM | CMOS/epi | MTA | 2Kx8 | — | 1.2E-2 (LET=20) | 70 (LET=20) | GSI Microprobe | No LU> 20 Metzger et al, RADECS92 |
| 9 | ESA | MHS65162 | SRAM | CMOS/epi (10 micron) | MTA | 2Kx8 | | 2E-2 (LET=35) | — | GSI SIS | No LU>35 Dreute, RADECS91 & 93 High vs lower energy comparison |
| 9 | CERT | HM65641 | SRAM | | MTA | 8Kx8 | | 0.2 | — | IPN | No LU>72 Falguere, RADECS91. p479 |
| 9 | CNES | HM65656 | SRAM | SOMOS/epi (high-performance) | MTA | 32Kx8 | [illegible] | 0.1 | 300 | IPN | Ecoffet et al IEEE92 prepr [illegible] data exists Date Code ES |
| 9 | ESA | MHS65664 | SRAM | CMOS/epi (5 microns) | MTA | 8Kx8 | <10 | 1.2E-2 | — | GSI S'S | No LU >35 Dreute et al, RADECS93 |
| 9 | CERT | HM65664 | SRAM | — | MTA | 8Kx8 | 5 | 0.4 | — | IPN | No LU>55 Falguere, RADECS91 p 479 |
| 9 | CNES | D431000 | SRAM | — | NEC | 128Kx8 | <3 | — | Double hits | IPN | Ecoffet et al, IEEE93 Workshop Proton data exists Date Code 9137 |
| 9 | CNES | D43256 | SRAM | — | NEC | 32Kx8 | <3 | — | Double hits | IPN | Ecoffet et al, IEEE93 Workshop Proton data exists Date Code 9035 |
| 9 | A | UPD43256A | SRAM | CMOS/NMOS | NEC | 32Kx8 | 3 | 0.4 | — | 88-in | No latchup March, 90 |
| 9 | CNES | CXK581000 | SRAM | DC 9252 | SNY | 128Kx8 | <1.7 | | 0.7 to 7 (pattern dependent) | IPN | Ecoffet et al, IEEE93 preprint Proton data exists |
| 9 | J | CXK581000P-10LL | SRAM | CMOS/NMOS | SNY | 128Kx8 | 1.4 | 0.18 | suggests multiple errors | BNL | LU(th) between 15 & 38 Mar '93 |
| 9 | CNES | CXK581001 | SRAM | DC 9150/9151 | SNY | 128Kx8 | <1 | — | 0.2 to 4 (pattern dependent) | IPN | Ecoffet et d, IEEE93 preprint Proton data exists |
| 9 | CNES | CXK58257 | SRAM | — | SNY | | <3 | — | — | IPN | Ecoffet et al, IEEE93 preprint Proton data exists |
| 9 | MVS | SMJ44C251 | SRAM (Video) | CMOS-1 micron | TIX | 256Kx4 | 05 | — | 120 | MVS/GAN'L | No LU>46 Beaucour, IEEE93 Workship, 7/93 |
| 9 | IBM | IMS16-1EPI | SRAM | CMOS/epi | TMS(1) | | 3 | 0.3 | | 88 in | No LU>60 T Scott 6/88 Proton data exists [1 1. SGS Thomson |
| 9 | R | UT67164 | SRAM | CMOS "prototype flow" | UTM | 8Kx8 | >37 | No upset | No upset | BNL | No LU >37 DC 9320 Bob Ferdon 7/10/93 |
| 10 | GDD | MB8116400-60PJ | DRAM | CMOS | FUJ | 4Mx4 | <1.4 | 3.5 | | BNL | No LU>80 SEFI at LET~50 LaBel test 5/94 |
| 10 | CNES | 01G9274 | DRAM | Date Code: ES | IBM | 1Mx4 | 2.5 | — | 2.4 | IPN | No LU Ecoffet et al, IEEE93 Proton data exists |
| 10 | J/Loral | LUNA-C DD3 | DRAM | CMOS/epi with ECC-- off | IBM | 4Mx4 | 4 @ 3.14V | — | 2 | BNL | No LU >120 @ 3 42V T Scott, Loral Internal Rept #94-GW3 008 (8/31/94) |
| 10 | CNES/ALC | LUNA-C | DRAM | CMOS/epi with ECC-- off or on | IBM | 4Mx4 | ~3 @ 3.6V | ~0.2 ECC off, 3E-3 on | — | BNL & IPN | No LU>120 Row & column errors unaff ected by ECC Calvel, IEEE94 |
| 10 | CNES/ALC | LUNA-E | DRAM | CMOS/epi without ECC | IBM | 4Mx4 | ~3 @ 5V | ~0.1 | — | BNL & IPN | No LU> 1 20 Row & column errors cross sections Compare above Calvel, IEEE94 |
| 10 | ESA | MT4C4001JC | DRAM | engr sample-shrunk 0.6mic line | MCN | 1Mx4 | ~1.5 | — | 40 to 80 | IPN | NO LU>120 DC 9244 Process D159 Harboe Sorensen, RADECS93, p490 |
| 10 | CNES | MT4C4001 | DRAM | DC 9109 & 9248 | MCN | 1Mx4 | <0.4 to <1.7 | — | 50 to 150 | IPN | No LU Ecoffet IEEE93 Workshop Stuck bits Proton data exist |
| 10 | GDD | MT4CM4B1DW | DRAM | CMOS | MCN | 4Mx4 | <1.4 | LU obscures it | — | BNL | LU 12 to 25, 2E-4cm2 LaBel Test 5/94 |
| 10 | J/TRW | — | DRAM | — | OKI | 4M | <1 | — | ~50 | BNL/88 in | N o LU>60 SEFI LET(th)=16, 700 sq mic [F/F model G Swift 94 SEU Symp |
| 10 | GDD | KM44C4000AJ7 | DRAM | CMOS | SAM | 4Mx4 | <1.46 | — | 17 | BNL | No LU>110 Stuck bits & SEFI at LET>60 DC 408Y LaBel 7/94 |
| 10 | IBM | SMJ27C128 25 | DRAM | CMOS | TIX | 16Kx8 | Rates given | — | — | BNL | The data here were taken as a subset of the TIX SM320E15 DSP 5/93 |
| 10 | IBM | 44400 | DRAM | | TIX | 1Mx4 | — | — | | BNL | No LU Soft error data exist Proton upset data exist T Scott, 1990 |
| 10 | CNES | SMJ44100 | DRAM | Date Code: ES | TIX | 4Mx1 | <0.4 | — | >24 | IPN | No LU Ecoffet et al IEEE93 Proton data exists See preceding entry |

Table 1 SEU Data

| | Test Org * | Device | Function | Technology | Mfr | Bits | Effective LET** Threshold | Device Cross Section (cm2)*** | Cross Section Per Bit (sq mic) | Facility **** | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | CNES/ALC | TMS416400-Rev. B | DRAM | CMOS/epi(0.5 mic) | TIX | 4Mx4 | <<1.7 | 5 | Full row errors =1E-4 cm2 | BNL & IPN | No LU>57. Functionality loss LET=25;5E-5 cm2. Half row errors. Calvet, IEEE94 |
| 10 | IBM | SMJ416400-1 thru-6 | DRAM | CMOS epi? | TIX | 4Mx4 | 0.4 | — | 1.1 | BNL | No LU LET>70. Functional loss LET(th)=12;2.7E-6 cm2. WP-2 (Pollock) 1/93 |
| 10 | GDD | TC5117400FT-70 | DRAM | CMOS | TOS | 4Mx4 | Inconsistent with previous test data. | | | BNL | Pending analysis. LaBel 5/94 |
| 10 | GDD | TC5117400J-6 | DRAM | CMOS | TOS | 4Mx4 | <1.46 | — | 18 | BNL | No LU>110. No stuck bits. No multiple errors. DC: Y60927. LaBel 7/94 |
| 12 | R | R29791 | PROM | Bipolar | RAY | 8Kx8 | 15 | 2.4E-5 | — | BNL | No LU>74 4/93 Upsets are transients at output; not lost data |
| 12 | | HS-6664PH | PROM (Fusible link) | CMOS, TSOS-4 process | HAR | 8Kx8 | >116 (test for data latches only) | | — | BNL | No LU>11 5 A, at 45 deg angle Harris Space Product News, 3rd Q, 1994 |
| 12 | J | 28C256 | EEPROM | CMOS | ATM | 32Kx8 | 3(read) | start/stop runaways at LET>16 | | BNL | Stuck bits (write) @ LET>50 SEU @ LET>3 (worst case "read") 1/94 |
| 12 | ESA | HN58C66P-25 | EEPROM | — | HTC | 8Kx8 | 7 to 11 (write); 53 (read) | 6E-4 (write) | — | BNL | No LU>84 Harboe-Sorensen, IEEE94 preprint Compared to flight data |
| 12 | ESA | HN58C256P-20 | EEPROM | Dia58C256R | HTC | 32Kx8 | 7 (write) | 4E-4 | — | BNL | No LU>53 DC 9232 Harboe-Sorensen, RADECS93 p 490 Compare SE(3 |
| 12 | NASA | DPZ128x16A3 | EEPROM (Flash) | Two 528%/3 dice | HTC | 256Kx8 | Only latchup was observed. | | — | BNL | LU(th)=20, 1 E-4 cm2 No current 5/93 Pat O'Neill Part listed as "Dense Pack" |
| 12 | MMS | MEM8129 | EEPROM | Bulk CMOS with MNOS | HTC(1) | 1M | 4 to 10 | 1E-3(critical errors for worst case "write") | Byte group errors | GAN'L | No LU>80 (1) by Hybrid Memory No hard errors DC 9322 Poivey, IEEE94 |
| 12 | GDD | HN58C1001 | EEPROM | CMOS/epi | HTC | 128Kx8 | 18 (write); >80 (read) | — | 0.4 per byte | BNL | No LU>90 LaBel 11/94 & 1/95 |
| 12 | NASA | FM1208S | EEPROM | TTL/CMOS | RVT | 512x8 | 20 | 2E-4 | — | BNL | LU(th ).25, 1 E 4 cm2 5/93 Pat M O'Neill (NASA-Johnson) |
| 12 | NASA | KM29C010 | EEPROM | CMOS | SAM | 128Kx8 | <<12 | 2.00E-02 | | BNL | No LU>45 5/93 P M O'Neill (NASA-Johnson) |
| 12 | J | 28C256 | EEPROM | CMOS/epi | SEQ | 32Kx8 | ~3 (write); 7(read) | 5E-2(write);2E-4(read) | — | BNL | Perm fail LET=60; 1/94 Byte autoerasures -- part of read mode @ LET~4, 12/94 |
| 12 | GDD | 28C256A | EEPROM | CMOS "5,2 | SEQ/SEI | 32Kx8 | 15 to 26 (LU & soft error) | — | — | BNL | LU at 1 5 to 26 HMC DC9224 in SEI package LaBel & Seidlick, 1/95 |
| 12 | GDD | 28C256E | EEPROM | CMOS/epi SGN's Rev. J | SEQ/SEI | 32Kx8 | 7(write);11 (read) | 5E-3 (write) | 8 | BNL | No LU>90 Perm write failure LET=60;1 E-5 cm2 SGN DC94367/92,11/94 & 1/95 |
| 12 | DASA/ESA | 28C256-200 | EEPROM | CMOS/18mic epi (SGN P402) | SEQ | 32Kx8 | 3(write) | 1.5E-3 (write) | — | BNL | No LU>74 Harboe- Sorensen "Read" is much less sensitive Nov 93 |
| 12 | ESA | 57C53B-5001 | EEPROM | CMOS p5,2 | SEQ | 32Kx8 | ~7(write) | >5E-5 (write) @ LET=26 | — | BNL | LU(th)=26(read); 5E-5cm2 DC 92239 Harboe Sorensen, RADECS93 preprint |
| 12 | MMS | 28C010 | EEPROM | CMOS bulk (FLOTEX) | SEQ | 128Kx8 | 4 to 10 | 1E-4 (critical errors--worst case "write") | 4% are page errors | GAN'L | LU(th)=32,5E-5 cm2 Poivey, IEEE94 DC 9334 Hard errors at LET=16 SEGR? |
| 12 | NASA | CQ28C010 | EEPROM | Cues P512 | SEQ | 128Kx8 | Only latchup observed | | — | BNL | LU(th) =22; ~ 1E-4 cm2 5/93 Pat M O'Neill 400 mA latchup currents |
| 12 | NASA | WE-512K8-150CX | EEPROM | CMOS P512 | SEQ(White) | Four 128Kx8 dies | Only latchup observed | | — | BNL | Latchup-like response @ LET(th)=20~1 E-69'112 5/93 P O'Neill (NASA-Johnson) |
| 12 | SNL | SA3923 | EEPROM | CMOS/SNOS (SNL design) | WEC | 8Kx8 | ~35 | 1E-5 (W C write (data) | — | BNL | No LU Hard errors at LET=40 in write mode Sexton, IEEE94 Workshop |
| 12 | IBM | 55C65 | EEPROM | CMOS | SEQ | 8Kx8 | 11 | 8E-4 | — | BNL | No LU>120 T Scott, 1990 Also Oct 1992 |
| 12 | IBM | 27C210 | UVEPROM | CMOS | INT | 64Kx16 | >6 | — | — | BNL | LU--Threshold not given; destructive at 09A T Scott, IBM Letter 1/93 |
| 14 | MMS | 1020 ?? | Field Prog. Gate Array | CMOS/epi (1.2 mic feature) | ACT | | 24 | N/A | 25 | MMS/GAN'L | No LU>76 Beaucour, IEEE93 Workshop 7/93 |
| 14 | A | A1020A | Field Prog. Gate Array | CMOS/epi (1.2 mic feature) | ACT | | 25 | N/A | 300 | 88 in | No LU>120 Koga, 94 SEE Symposium |
| 14 | A | A1020B | Field Prog. Gate Array | CMOS/epi (1.0 mic feature) | ACT | 200 F/F | ~10 | 1E-3 per 200 F/F's | 300 | 88 in | LU(th)=55;2E-5cm2 Ma Tsuchita dice Koga 94 SEE Symposium |
| 14 | JH | A1280 | Field Prog. Gate Array | CMOS/epi (1.2 mic feature) | ACT | 4 tests/552 mods | 25(C), 5(S) | 4E-5 cm2 output latch | 600(S) & 100(C) per module | BNL | No LU>76 Priscilla McKerracher(JH) & Rich Katz(Goddard) 11/93 |
| 14 | A/GDD | A1280A | Field Prog. Gate Array | CMOS/epi (1.0 mic feature) | ACT | 1232 modules | 28(C), 5(S) | — | 800(S) & 200(C) | 88-in | A: No LU>100 ACT II C=combinatorial, S=sequential logic Koga 93 GDD 2/94 |
| 14 | IBM | 7256GC192-2 | Field Prog. Gate Array | | ALT | — | Rates given. | — | — | BNL | Latchup rates given 5/93 DC 9249 WP-2 (Jim Pollack) |
| 14 | GDD | CP20420 | Field Prog. Gate Array | CMOS | CPT | — | ~12.5 | — | 0.02 | BNL | LU @ 15-27 LaBel, 94 IEEE Workshop Record |
| 14 | HAR | 3020 | Field Prog. Gate Array | Rad Hard CMOS/SOI | HAR | — | 100 | — | 1E-3 | BNL | No LU>120 (Au only) Harris Development Package, 5/93 |
| 14 | HAR | 3090 | Field Prog. Gate Array | Rad Hard CMOS/SOI | HAR | ~50,000 | 100 | — | 1E-3 | BNL | No LU>120 (Au only) Harris Development Package, 5/93 |
| 14 | J | HR1000 | Gate Array (custom CDU) | RICMOS III | HON | RAM+special tests | 60 | Not available | Not available | BNL | No LU>120 to 125 deg C Same fab, different implementation as above 3/94 |
| 14 | GDD | HR2340 | Gate Array (multifunctions) | RICMOS IV | HON | soft latch & RH | 16(soft latch); 60 (rad hard) | | 100 200 (soft latch); 25 (rad hard) | BNL | |
| 14 | HAC | LCA200K Process | ASIC Process test chip | 200K series ASIC process | LSI | — | 5(LU masks SEU) | 0.04 | | 88-in | LU=5 @ 37 deg. & 3.2 @ 60 deg. C LU doesn't damage device Shoga 3/93 |
| 14 | J | LCA10038Q | Process Prog. GA | HCMOS/epi (1.0 mic)-- not RH | LSI | 64-bit RAM only | 30 | N/A | 200 | BNL | No LU>115 July 1993 Only 64-bit RAM tested |
| 14 | MMS | TPC1020 | Field Prog. Gate Array | CMOS/epi (1.2 mic feature) | TIX | — | 20 | — | 20 | MMS/GAN'L | No LU>76 Beaucour, IEEE93 Workshop 7/93 |
| 14 | UTM | UTE-R 50K | Gate Array | CMOS/epi (5 mic) | UTM | 4K SRAM | ~36 | — | 130-180 | BNL | No LU> 165 6/93 |
| 14 | UTM | UTE-R 75K | Gate Array | CMOS/epi (3 metal overlayer) | UTM | 1K SRAM config. | 36 | — | , 500 per cell | BNL | No LU Runaway in F/F support circuitry Rudeck, 12/93 |
| 14 | IBM | RHCMOS2 | Expressway GA | CMOS | IBM | 2587 | >6 | — | — | BNL | No LU>120 1/93 T. Scott, IBM Letter |
| 14 | IBM | BTVCMOS2 | SPD3 Gate Array | CMOS II (Burlington, VT) | IBM | — | 3 | — | 90 | BNL | LU=25; LU rates given by J Pollock of WP-2 Tested 1/93 by T Scott |
| 15 | Soreq, Isr | PAL16R8BMJ/883B | PLA | Bipolar (two parts) | AMD | — | 7 (WC1's) | 2.50E-04 | 1000(2) | Van de G (1) | J Barak, IEEE93 preprint Test 8 M reg (1)=Weizmann Inst Israel (2)=gates |
| 15 | GDD | AT22V10 | PLA | CMOS | ATM | — | ~10 | 3E-5 | | BNL | No LU>80 Tested 8/93 LaBel, 94 IEEE Workshop Record |
| 15 | MMS | TIBPAL22V10 | PLA | Bipolar | TIX | — | 9 | — | 2000 | GAN'L | No LU> 140 Beaucour, IEEE93 Workshop & July 94 |
| 15 | ESA/MMS | 22V10 | PLA | Bipolar IMPACT | TIX | — | — | 2E-5 | — | GAN'L | No LU H Van Looy ESA Rept 1 9 9 3 |
| 15 | ESA/MMS | 16L8 | PLA | Bipolar IMPACT | TIX | — | — | , 3E-5 | — | GAN'L | No LU H Van Looy ESA Rept 1993 |
| 15 | MMS | TIBPAL16R8 | PLA | Bipolar | TIX | — | 0 | — | 1100 | GAN'L | No LU>140 Beaucour, IEEE93 Workshop & July 94 |
| 15 | BDS/McD | EP610 | Electronically PLD | CMOS bulk | ALT | — | — | — | | 88-in | LU=9,5E-4cm2 DC9317, Temp = 44 to 100 deg C E Normand (BREL) 10/94 |
| 15 | McD | EP1810 | Electronically PLD | CMOS bulk | ALT | — | <4 | 0.01 | — | 88-in | LU=~5;1E-3cm2 W Zakrzewski, 9/93 (Also tested EP610) |
| 15 | PHY | EPM5032 | UVE Electronically PLD | CMOS bulk | ALT | — | Soft errors were masked by latchup. | | — | 9 NL | LU=~3;1E 3 cm2 Temp = 95 deg C Rept No PHY 93R013 (3/11/93) |
| 15 | IBM | CY-7C344 | Electronically PLD | CMOS bulk | CY P | — | ? | Rates given | | BNL | Latchup rates given April 93 DC 9305 WP-2 (Jim Pollack) |
| 16 | GDD | 1XD3-0701 | RS Encoder-DataCommand | Rad Hard CMOS/epi | UTM | — | 38 | 55E-4 @ LET=120 | — | BNL | No LU>120 LaBel, 93 IEEE Workshop Record |
| 16 | J | AACS/OU Custom | 1553 Interface | CMOS/epi gate array | UTM | Man Enc/dec only | 60 | 1E-5 @ LET=120 | — | BNL | No LU >120 at 125 deg C 3/93 |
| 17 | GDD | IDT49C460 | EDAC (32 bit) | CMOS | IDT | — | 15 to 20 | 5E-5 (total error types) | — | BNL | No LU >80 Five different error types were monitored LaBel 1 1/94 |
| 18 | GDD | Hot Rod TX | Transmitter/Receiver pair | GaAs | GAZ | — | <14 | ? E-3 | — | BNL | No LU>120 LaBel, IEEE93 & 94 Workshop Proton data exist |
| 18 | GDD | Hot Rod REC | Transmitter/Receiver pair | GaAs | GAZ | — | <14 | 1 5 E-3 | — | BNL | No LU>120 LaBel, IEEE93 & 94 Workshop Proton data exist |
| 18 | GDD | TAXI | Transmitter/Receiver pair | Bipolar | AMD | — | — | — | — | BNL | No LU >50 7/93 LaBel, IEEE93 Workshop Record |
| 18 | GDD | AX3411 | 1553B Transceiver 15V | Bipolar | AFX | — | <115 | ? E-4 @ LET=80 | — | BNL | No LU>80 8/93 & LaBel 94 IEEE Workshop Record DC A67625 |

Table 1 SEU Data

| | Test Org * | Device | Function | Technology | Mfr. | Bits | Effective LET** Threshold | Device Cross Section (cm2)*** | Cross Section Per Bit (sq mic) | Facility **** | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 18 | GDD | AX3453 | 1553B Transceiver 5V | Bipolar | AEX | — | <11.5 | 5 E-5 @ LET=80 | — | BNL | No LU>80 8/93 & LaBel 94IEEE Workshop Record |
| 18 | GDD | DDC63125 (ILC) | 1553B Transceiver 15V | Bipolar | DDC | — | 14 | 3 E-4 | — | BNL | No LU>80 8/93 & LaBel 94IEEE WorkshopRecord |
| 18 | GDD | 74FTC163245PV | 3.3V/5V Transceiver | CEMOS (low power) | IDT | — | None at LET< latchup threshold | | | BNL | LU=25; 5E-4 cm2/device Compare to IDT CEMOS register LaBel test d 5/94 |
| 18 | HON | LTC485 | RS485 Transceiver | CMOS | LTN | no latches | — | — | — | BNL | LU(th)=1 4.1 3E-5cm2 DC9227 WP2(Jim Pollock) 8/93 |
| 18 | GDD | CT1497D | 1553B Transceiver 15V | Bipolar | MED | ■ | 11.5 | 5.5 E-5 | — | BNL | No LU>80 9,93 LaBel 94 IEEE Workshop RecordDC 9316 |
| 18 | GDD | CT2521 | 1553B Transceiver 5V | Bipolar | MED | — | <26.5 | 4.5 E-4 | — | BNL | No LU>80 8/93 LaBel Test Rept & 94IEEE WR DC 9249 DUTs "failed" with Ni |
| 18 | GDD | NH1500 | 1553B Transceiver 15V | Bipolar-- National Hybrids | NSC | — | <11.5 | 6 E-6 | — | BNL | No LU>80 8/93 LaBel Test Reel 6 94IEEE W?? DC 9328 Die bigger than beam |
| 18 | GDD | NH1529 | 1553B Transceiver 5V | Bipolar-- National Hybrids | NSC | — | <11.5 | 1.5 E-5 | — | BNL | No LU>80 8/93 LaBel Test Rept & 94IEEE WR DC 9329 |
| 18 | GDD | FC1553921 | 1553B Transceiver 5V | Bipolar | STC | — | <11.5 | 2 E-3 | | BNL | No LU>80 8/93 La Bel Test Rept & 94 I EEE WR OuTs "failed" with Ni |
| 18 | GDD | UTMC63M125 | 1553 bus transceiver | Bipolar | UTM | — | 11 | TBD | — | 9NL | LU(th )=27 with one maverick LU at LET. 11M Gales 6/93 |
| 18 | GDD | UT53M125 | 1553B Transceiver 15V | Bipolar | UTM | — | <11.5 | 3E-4 @ LET=80 | — | BNL | No LU>80 8/93 LaBel Test Rept & 94IEEE WR DC 92 50/9315 |
| 18 | GDD | M63147 | 1553B Transceiver 5V | Bipolar | UTM/MR | — | <11.5 | 1 E-4 | — | BNL | No LU>80 8/93 LaBel Test Rept & 94IEEE WR Hi Rel samples |
| 18 | ADI | AD8001 | Op Amp | Bipolar-XFCB process | ADI | — | >82 | Depends on discrimination level | | BNL | No LU>82 M DeLaus, 94IEEE Workshop Record |
| 18 | A | HS3530RH | Op Amp | rad hard | HAR | — | Cross sections & thresholds depend on amplitude discrimination voltages. | | | 88-In | No LU Refer to Koga et al, IEEE. NS, p1838 (Dec 93) DC8839 |
| 18 | CNES/A | LM108 | Op Amp | | MOT | — | -2 | Depends on discrimination level | | IPN | No LU>27 Ecoffet et al, 94 IEEE Worskhop Record |
| 18 | GDD | LM108 | Op Amp | Bipolar | NSC | — | <25 | — | — | BNL | TID degradation at <2.5 krad obscured SEE data LaBel, IEEE Workshop 1994 |
| 18 | GDD | LM124 | Op Amp | Bipolar | NSC | — | — | — | — | BNL | No LU>90 DC: B9412AD LaBel 6/94 |
| 18 | GDD | LM158 | Op Amp | Bipolar | NSC | — | — | — | — | BNL | No LU>100 DC AA04324587 LaBel 7/94. |
| 18 | CNES | LM218H | Op Amp | | NSC | — | This fast op amp has a greater cross section than MOT LM108. | | | CI-252 | No LU>27 Ecoffet et al, 94 IEEE Worskhop Record |
| 18 | GDD | LM108AH | Op Amp | Bipolar | PMI | — | 24 | 5E-4 | — | BNL | LU=-60 Date Code: B9412AD LaBel 6/94 |
| 18 | A | OP-05 | Op Amp | Bipolar | PMI | — | Cross sections & thresholds depend on amplitude discrimination voltages. | | | 88-In | No LU Refer to Koga et al, IEEE- NS, p1838 (Dec 93) DC9206 |
| 18 | GDD | OP-07AJ | Op Amp | Bipolar | PMI | — | 12 | 3E-4 | — | BNL | No LU>50 DC 9345 Test, LaBel 6/94 |
| 18 | A | OP-15 | Op Amp | Bipolar | PMI | Cross sections & thresholds depend on amplitude discrimination voltages. | | | | 881" | No LU Refer to Koga et al, IEEE-NS, p 1838 (Dec 93) DC9246 |
| 18 | GDD | OP-97 | Op Amp | Bipolar | PMI | — | — | — | — | BNL | No LU> 1 10 DC unknown La Bel 7/94 |
| 18 | GDD | SMP11 | Op Amp | Bipolar-Super Beta transistors | PMI | — | | — | — | BNL | No LU>80 None were functional post test DC 085 LaBel 7/94 |
| 18 | GDD | EL2243 | Analog Op Amp | Bipolar | ELJ | — | 5 | 1 E-3 | — | BNL | No LU>90 LaBel, 94IEEE Workshop Record Tested 5/93 |
| 18 | GDD | PA10 | Power Op Amp | Bipolar | APX | — | — | — | — | BNL | No LU>100 OC VE1009321 Test, LaBel (7/94) |
| 18 | GDD | AD524 | Diff amplifier | Bipolar | ADI | — | 12 | 1E-2 | | BNL | No LU>80 DC 9364 LaBel 6/94 |
| 18 | GDD | LM120H-12/883C | Voltage regulator | Bipolar | NSC | — | — | — | | BNL | No LU>110 OC H2C9 327A LaBel 7/94 |
| 18 | GDD | LM117H | Voltage regulator | Bipolar | NSC | — | — | — | — | BNL | No LU>110 OC C92 LaBel 7/94 |
| 18 | GDD | LM136AH | Voltage regulator | Bipolar | NSC | — | | — | | [illegible] | No [illegible] 10 DC 9320 LaBel 7/94 |
| 18 | GDD | LP2951 | Voltage regulator | | NSC | — | <25 | — | — | BNL | No LU>90 LaBel 11/94 |
| 18 | GDD | REF-02-373J | Voltage reference | Bipolar | PMI | — | — | — | — | BNL | No LU, 100 DC Q8573944 Test, LaBel 7/94 |
| 18 | GDD | SE5521F | Signal conditioner | Bipolar | SGN | — | — | — | — | BNL | No LU>100 DC 012BD19-9401RD Test, LaBel 7/94 |
| 18 | CNES | LM111 | Voltage Comparator | — | MOT | — | .2 (transients >2.4V) Depends on discrimination level | | | IPN | No LU>27 Ecoffet et al, 94 IEEE Worskhop Record |
| 18 | A | LM111H | Voltage Comparator | Bipolar | N SC | — | .5 for discriminator set at -1 V Would be much lower at lower V | | | 88-In | No LU Refer to Koga et al, IEEE NS, p1838 (Dec 93) DC9151 |
| 18 | GDD | LM119 | Comparator | Bipolar | NSC | — | — | — | — | BNL | No LU> 1 . 0 for 1E6 ions/cm2 LaBel 7/94 DC 88305 |
| 18 | GDD | LM193H | Comparator | Bipolar | NSC | | — | — | — | BNL | No LU>100 for 1E6 ions/cm2 LaBel 7/94 DC 29344A |
| 18 | GDD | LM139 | Comparator | Bipolar | NSC | | 50 | 2E-5 @ LET=100 | — | BNL | Perm current decrease at LET=82 LaBel, Jan & Feb 94 |
| 18 | GDD | LM139A | Comparator | Bipolar | NSC | — | — | — | — | BNL | No LU>80 DC 9412 LaBel 6/94 |
| 18 | GDD | IDA0731R | Laser Driver | | HPA | — | — | — | — | BNL | No LU>80 LaBel Test Rept 8/93 |
| 18 | GDD | 88C20 | Diff Line receiver | CMOS | NSC | — | 11 | 1E-5 | — | 9NL | No LU>100 1/94 LaBel, 94 SEE Symposium |
| 18 | GDD | 88C30 | Diff Line driver | CMOS | NSC | — | >120 | — | — | BNL | No LU>120 1/94 LaBel, 94 SEE Symposium |
| 18 | GDD | TSC4429 | MOSFET driver | — | TEL | — | >120 | — | — | BNL | No LU> 120 Tested1/94 LaBel, 94IEEE Workshop Record |
| 18 | ESA | D469A | High Current Power Driver | CMOS/epi (PolyMOS) | SIL | — | — | — | — | GANIL | LU(th) =51; 9E-5 cm2 H Van Looy, ESA Rept 1993 |
| 18 | J | MIC4420 | Buffer driver | No memoryelements | MIC | — | — | — | — | BNL | No LU>120 8/92 Includes temp up to 125 deg C |
| 18 | J/GDD | HS26C31 | Diff Line driver | HCMOS/SOS | HAR | — | >80 | — | — | BNL | J No LU >120 up to 100 deg C 9/92 GDD Test 5/93 La Bel 94IEEE Workshop |
| 18 | J/GDD | HS26C32 | Diff Line receiver | HCMOS/SOS | HAR | — | >80 | | — | BNL | J No LU >,20 up to 100 deg C 9,92 GDD Test 5/93 LaBel 94IEEE Workshop |
| 18 | BPS | 26C31 | Linedriver | CMOS | NSC | — | — | — | — | UW? | Latchup rate reported but no threshold June 93 WP-01 Wes Will |
| 18 | BPS | 26C32 | Linereceiver | cMOS | NSC | — | — | — | — | UW? | Latchup rate reported but no threshold June 93 WP-01; Wes Will |
| 18 | BPS | DG201(M38510) | SPST Switch | Unknown | HAR | — | — | — | — | UW? | No latchup @ LET=38 W Will, (WP-01) DC 9218 May 1993 |
| 18 | BPS | DG201(M38510) | SPST Switch | Unknown | SIL | | — | — | — | Uw? | No latchup @ LET=38 W Will (WP 01) DC 9125 May 1993 |
| 18 | BPS | DG507AAK/883 | Analog Switch | Unknown | SIL | | — | — | — | UW? | No latchup @ LET=38 W Will (WP 01) DC 9134 May 1993 |
| 19 | MM | CA3338AD | DAC (8 bit) | CMOS/TTL | HAR | — | >11.9 | — | — | BNL | No LU>119 DC 9307 T Rao-Sahib for WP 02 5/1.393 |
| 19 | GDD | DAC08AQ | DAC (8-bit) | Bipolar | PMI | — | -35150 mV transients! | 2E-2 (50 mV transients! | — | BNL | No LU>80 Cross section depends on transient size DC9220A LaBel 7/94 |
| 19 | GDD | AD565 | DAC (12 bit) | Bipolar | ADI | — | — | — | — | BNL | No LU>80 DC 9145 LaBel 17,"34 |
| 19 | J | AD7545AKN | DAC (12 bit) | CMOS | ADI | — | >120 (all 1's only) | — | — | BNL | No LU>120 Up to 80 deg C Nichols, Feb & April, 95 |
| 19 | J | HAR7574KN | DAC (12-bit) | CMOS | HAR | — | — | — | — | BNL | No LU>120 Up to 80 deg C Nichols, Feb 1995 |
| 19' | | MX7545TQ | DAC (12 bit) | CMOS | MAX | — | >120 (all 1's only) | — | — | BNL | No Lu> 120 April 95 |
| 19 | J | MP7545TD/883 | DAC (12 bit) | CMOS | MPS | — | >120 (all 1's only) | — | — | BNL | No LU>120 Up to 80 deg C Nichols, Feb & April, 95 |
| 19 | J | MP7545/TD883 | DAC (12 bit) | CMOS | MPS | — | > 120 (all 1's only) | — | — | BNL | N o LU> 120 Up to 80 deg C Nichols, Feb & April 95 |
| , 9 | GDD | 7820RP/372 | A/D (8 bit) | LCCMOS (Seiko 0820 die) | MPS | | — | — | — | BNL | No LU>80 LaBel 7/94 |
| 19 | A | TDC1048 | A/D (8 bit) | Bipolar hybrid | TRw | — | 2 | 2E-3 | | 88in | No LU LET >95 DC 8540 4/93 |
| 19 | A | AD9048 | A/D (8 bit Flash) | Bipolar | ADI | — | <1 | 2E 4 | — | 88 in | Fail to 2's complement @ LET=8.1 5E 5 cm2 DC 9145 Koga IEEE94, p2172 |

Table 1. SEU Data

| | Test Org * | Device | Function | Technology | Mfr. | Bits | Effective LET** Threshold | Device Cross Section (cm2)*** | Cross Section Per Bit (sq mic) | Facility **** | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 19 | SNL | HS9008RH | A/D (8-bit Flash) | CMOS | HAR | — | ~15 | 2E-5 | — | BNL | No LU>150 to T=125 deg C No temp dependence Se xton, IEEE94 Workshop |
| 19 | GDD | AD1671JD | A/D (12-bit) | Bipolar/CMOS | ADI | — | | — | — | BNL | No LU >90 A. K Moran 4/93 & LaBel 94IEEE Workshop Record DC9219 |
| 19 | BDS | AD7541 ATQ/883B | A/D (12-bit) | — | ADI | — | — | — | — | 88-in | No LU>38 5 w Will (WP-01) DC 9139 May 93 |
| ,9 | J | AD7870 | A/D (12-bit) | LCCMOS non hard | ADI | — | — | — | — | BNL | No LU>120 Nichols for SBRC Up to 60 deg C IEEE95 |
| 19 | SNL | AD7876 | A/D (12-bit) | LCCMOS new%.d | ADI | — | 2 | 2E-3 | — | BNL | No LU>150 Sexton IEEE94 Workshop Record, p55 |
| 19 | NWSC & A | AD42961 (hard AD871) | A/D (12 bit) | RBCMOS (rad-hard) | ADI | | 5 | 1.8E-5 ( offset errors, per million samples) | | 88-in | No LU>120 Noise error cross section = 1 E-5 cm2/MS Turflinger, IEEE-NS 94 |
| 19 | NWSC | RBC- 12 (hard AD872) | A/D (12-bit) | RBCMOS (rad-hard) | ADI | — | 5 | 1.8E-5 ( offset errors, per million samples) | | 88-in | No LU>120 Noise error cross section = 1 E-5 cm2/MS Turflinger, IEEE-NS 94 |
| 19 | J/HON | HI574 | A/D (12-bit) | CMOS | HAR | — | 10 | 8E-5 | — | BNL | *J No LU>120, 12/94, HON SEU data, DC9210, 10/92 |
| 19 | GDD | SPT7922 | A/D (12-bit) | Bipolar | SGP | | ≤3.4 | 1.5E-3 (delta V = 55mV) | — | BNL | No LU>120 LaBel, 94 IEEE Workshop Record |
| 19 | GDD | HS5212 | A/D (12-bit) | Hybrid | SIP | — | ~1.4 | 1E-3 | — | BNL | No LU>80 LaBel 2/94 94SEE Symposium |
| 19 | HON | HS5214 | A/D (12-bit) | Bipolar hybrid | SIP | SAR only | <1 ! Parallel | 1.5E-3 | — | BNL | No LU>>37 Serial Mode; SEU LET(th)= 1 6, 2 9E-5 cm2 2/93 |
| 19 | HON | HS5214 (AD5214) | A/D (12-bit) | — | SIP | — | <1 ; Parallel | 1.5E-3 | — | BNL? | No LU ,37, DC 9247 2/16/93 |
| 19 | J | SP674AU/B | A/D (12-bit) | Some MOS | SIP | | — | — | — | BNL | LU(th) -26 with large variability Some soft error data 3/93 |
| 19 | GDD | AD676BD | A/D (16-bit) | Hybrid CMOS&BiMOS!! | ADI | — | <3.4 | Not obtained | — | BNL | LU(th)=25 LaBel, 94IEEE Workshop Record Tested 6/93 |
| 19 | Ball | AD677 | A/D (16-bit) | Hybrid CMOS & BiMOS !! | ADI | — | 34 | See IEEE paper (remarks) | | BNL | LU(th)=31 (self-correcting),5E-5 cm2 Compare AD676 D Wilson 0", IEEE94 |
| 19 | J | ADS7805 | A/D (16 bit) | CMOS/epi(7 mic ) | BUB | | | — | — | BNL | LU(th) <<38 12/94. |
| 19 | J/GDD | CS5327 | A/D (16 bit) stereo | CmoS (analog 6 digital chip) | CRY | — | 3 | 5E-3(W.C. digital chip) | — | BNL | No LU>I15 7/93 Digital more susceptible than analog chip 0 V input only |
| 19 | A | MAX195 | A/D (16-bit) | BiCMOS | MXM | — | — | | — | 88-in | LU(th)=40; 5E-5 cm2 Koga 1 984 |
| 19 | A | HS9576RH | A/D(16-bit) | CMOS Hybrid | SIP | — | 3 | 5E-4 | | 88-in | No LU >100 Jan 1592 |
| 20 | JH | ART2815T & family | DC/DC Power Converter | rad hard design!IC's etc! | ADA | — | >83 | — | — | BNL | No LU>83. Tested Feb 94. D. Myers, 94!EEE Workshop Record. |
| 20 | A | ATW28XX | DC/DC Converter module | CMOS (one IC) | ADA | — | — | — | | 88-in | LU(th)=51-80; ~1E-6cm2. Oct 1991 |
| 20 | GDD | MFL2815D | DC/DCPower Converter | — | ITP | | 451060 (voltage drop) | | — | BNL | No destructive cond. @ LET>72. 11/94 |
| 20 | GDD | MFL2815S | DC/DC Power Converter | — | ITP | | No transient errors >72 | | — | BNL | No destructive cond. @ LET>72. 11/94 |
| 20 | GDD | MFL2812S | DC/DC Prover Converter | — | ITP | — | 50 (voltage spikes) | 5E-6 | | BNL | Spikes are 0.6V, 5E-6 cm2, <20 nanos. No destructive cond. @LET>72. 11/94 |
| 20 | GDD | MFL2805 S | DC/DC Power Converter | — | ITP | — | No transient errors >72 | | — | BNL | No destructive cond. @ LET>72. 11/94 |
| 20 | GDD | 2690R-D15F | DC/DC Power converter | | MDI | — | 4 to 8 (reset errors) | 5E4 (reset errors) | — | BNL | No destructive cond. @ LET>72. 11/94 |
| 20 | GDD | AHE2815DF/CH-SLV | DC/DC Power Converter | Bipolar | ADA | | 20 (Switchoff error) 1 E., | | — | BNL | Destructive cond. @ LET=27 (SEGR?) Power MOSFET switching "on" (7/94) |
| 20 | GDD | AHE2815D/HB | DC/DCPowerConverter | Bipolar | ADA | — | 20 (Switchoff error) 1 E-4 | | | BNL | Destructive cond @ LET=27 (S EGR?) Power MOSFET switching "on" (1 1/94) |
| 21 | A | SP8908 | PLL Divide by eight | Bipolar-ECL HF process | GEC PLS | | | ~1E-4 | Not applicable | 88 - | Shoga, IEEE94-NS 2252 Sophisticated phase & amplitude measurements. |
| 21 | BPS | MC14515BP2 | PLL Freq. Synthesizer | Unknown See DC's. | MOT | — | 17+/-3 | 3E-4 | Not applicable | UW7 | No LU>38. 10/92 & 5/93 W. Will (WP-01). DC OY9141 & QQST9217 |
| 21 | IBM | WD33 92 A | SCSI Bus Controller | Unknown | WDC | .<37 | Rates given | — | — | BNL | No LU>37. 5/93. WP-2 (Jim Pollock) |
| 21 | IBM | ADS 10C00JT00 | Disk Controller | Unknown | WDC | <<37 | Rates given | — | — | BNL | No LU>37. 5/93. WP-2 (Jim Pollock) |
| 21 | GDD | SSP-21110-025 | Solid State Power Controller | Hybrid (ASICs, power FETs, etc.) | DDC | >80 | — | — | — | BNL | No transients, SEB, SEGR for LET>80. LaBel,Test 2/94 |
| 21 | GDD | HS2420 | Sample & Hold | HCMOS (1.2 mic) rad hard | HAR | | 20 | 5E-6 | — | BNL | No LU>80. LaBel 3/93 & 94!EEE Workshop Record. |
| 21 | J | DON688 | Power SCR | Discrete. BV=400V | SSD | | >60 !! at 0 and 60 deg ! | | | BNL | No SCR turn-on at LET=60 or effective LET=115. See following entry. 7/93 |
| 21 | J | D1777A | Power SCR | Discrete. BV=400V | SSD | — | >60 !! at 0 and 60 deg ! | | | BNL | No SCR turn-on at LET=60 or effective LET=115. See preceding entry. 7/93 |
| 21 | GDD | EMXO | Precision Oscillator | Hybrid Circuit | BAL | — | >85 | — | | BNL | No LU>85. 7/93. LaBel, IEEE93 Workshop Record |
| 21 | GDD | HFD3801-002 | Fiber Optic Receiver | TTL Integrated | HON | — | ~2 | 7E-2 | | BNL | LaBel, 12/90. Operated as pair with following entry. Proton data exists |
| 21 | GDD | HFE4811012 | Fiber Optic Transmitter | TTL Integrated | HON | | 13 | 3E-4 | | BNL | LaBel, 12/90. Operated as a pair with preceding entry. |
| 21 | GDD | ODL200TX | Fiber Optic Transceiver | Bipolar/GaAlAs | ATT | | 82>SEU>45 | | | BNL | No LU>82. Test 1/94. LaBel 94!EEE Workshop Record |
| 21 | GDD | ODL200 REC | Fiber Optic Receiver (diode) | Bipolar/GaAlAs | ATT | — | ~3 | 2.0 5E-4 (depends on clock rate) | | BNL | No LU> 82 Test 1/94 LaBel 94!EEE Workshop Record |
| 21 | J | 9407 | 4 Bit Data Reg. | Bipolar-TTL | FAS | 32 | <2.9 | 7 E-4 | 2200 | 88in | 4 registers |
| 21 | J | 9407 | 4-Bit Data Reg. | Bipolar-ITL | FAS | 32 | 15 | 1.4 E-4 | 400 | 88in | 4 registers Here ITL is seen to be harder than TTL (above ) |
| 21 | J | L29C520 | Pipelined Register | CMOS | LDI | — | — | | | BNL | LU(th) =26; 5E-5 cm2 3/93 |
| 21 | A | LTC1064 | Low Pass Filter | CMOS | LTN | — | | — | — | 88-in | LU(th)= 15; 3E-4 cm2 See following Dec 1592 |
| 21 | BPS | LTC1064 | Low Pass Filter | CMOS | LTN | — | | | — | Uw? | LU(th)=11; 1E-2 cm2 O LET=36 WP-01; Wes Will May 93 |
| 21 | CNES | SOR5053 | Coder | CMOS | SOR | | — | — | | IPN | LU(th) .9 Chapuis '90 |
| 21 | HON | AD2S80 | Resolver Dig. Conv. | — | ADI | — | 34 | — | 16, 000 (sat Worst Case) | BNL | No LU>37 DC 9227 2/17/93 |
| 21 | J | HSRD1056 | Resolver Dig. Conv. | Hybrid RH CMOS | NTL | 16 tested | ., 3 | SE-5 | — | BNL | No latchup LET>I10 Dec 1991 |

*J=JPL (D Nichols), A= Aerospace (R Koga) R=Rockwell or (RT ! J Pickel), SNL=Sandia, NTT=Nippon Tel & Tel Corp HAC= Hughes (El Segundo, CA) CNES=Centre National d Etudes Spatiales (France), GD=General Dynamics (J Elliott, SEE Symp '90),
ESA=European Space Agency HON=Honeywell, Saab= Saab Since (Sweden), HAR= Harris Corp Gov't Aerospace Systems Div Melbourne, FL LIN= Lincoln Labs-MIT (V Sferrino) NRL=Naval Research Laboratory (Washington D C)
BREL=Boeing Research Laboratories, Seattle, BDS=Boeing Defense & Space Group (Seattle), S3. S-Cubed (La Jolla, CA). Clem=Clemson University, MMS=Matra Marconi Space (France), HAC=Hughes Space & Communications (L A)
MM=Martin Marietta Astrospace (Valley Forge, PA), DASA=Deutsche Aerospace AG (Munich), GDD=NASA Goddard (K LaBel), NWSC=Naval Weapon Support Center (Crane, IN), CERT=ONERA/CERT (Space Technology Deed ] Toulouse France
MOT=Motorola GSIG (Tet Pang), LLNL=Lawrence Livermore Nat'l Lab (J R Kimbrough); ALC. Alcatel Espace (Toulouse) (P Calvel)
McD= McDonnell Douglas Huntington Beach, CA (Zakrzewski); PHY= Physitron, San Diego

**LET is effective (angle corrected) Linear Energy Transfer in MeV/(mg/cm2)

- - - Unless otherwise noted, the cross section (upsets/fluence per device) is given for 120-360 MeV Kr or Br ions at normal incidence, having an LET=37 MeV/(mg/cm2)
Cross sections for parts having LET>40 are typically for xenon or iodine ions and may include the effective LET of higher angle (grazing) ion incidence

****CIT is Cal Tech Van de Graaff; ORNL is Oak Ridge 75 MeV Tandem Van de Graaff; Cf-252 is any Cf-252 facility; GSI=German high energy cyclotron at Darmstadt; Orsay is French (IPN) cyclotron; BNL is Brookhaven National Laboratory Tandem Van de Graaff,
GANIL is Cyclotron at Caen, France; IPN is Tandem Van de Graaff at Institut Physique Nucleaire, Orsay France, UW is University of Washington Van de Graaff; other facilities are U C Berkeley cyclotrons