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Demonstration of 10 Kelvin Superconducting Electronics in an Infrared Imaging System

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We report the successful operation of a superconducting niobium nitride (NbN) Josephson Junction-based analog-to-digital converter (ADC) in an infrared imaging system. This system is a flexible testbed which will allow the evaluation of a large variety of cryogenic components (e.g. detector arrays, ADC's, etc.), while still following the general architecture of a scientific instrument, permitting us to determine how well the component will perform in the "real world". The testbed is currently composed of a Rockwell International HF-16 128x128 pixel Si:As BIB array, a JPL-developed GaAs 16-to-1 analog multiplexer, and a TRW 12-bit, 10 mega-samples per second, NbN ADC. All three components are located inside a pour/fill liquid helium dewar and operated at 10 K. Simple cold optics along with an 8.5 micron filter image objects onto the focal plane. The images are read out at rates up to 600 frames per second; data can either be stored to hard disk at this rate or every 20th frame can be displayed on a monitor providing "real-time" video. We describe the layout and operation of the testbed, with particular emphasis on the lessons learned about operating superconducting electronics as merely another component in a system. We also discuss images and other data comparing the performance of the NbN ADC with a commercially available, equal speed and resolution, silicon ADC. Finally, we explore the future of superconducting electronics; potential products as well as their impact on instrument and spacecraft design.

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JPL

General Overview

Conduct a system-level sensor demonstration of a very long wavelength infrared focal plane array, buffer electronics, and the TRW superconducting analog-to-digital converter operating at 10 Kelvin in a dewar environment.

Demonstration Goals:

ADC Goals

- Operating temperature of 10 Kelvin
- No missing codes in digitized data at 10 MHz input rate
- Noise performance at least as good as a Si ADC outside the dewar
- Power dissipation acceptable for space applications

System Goals:

- Real-time video display
- Relevant data processed within minutes

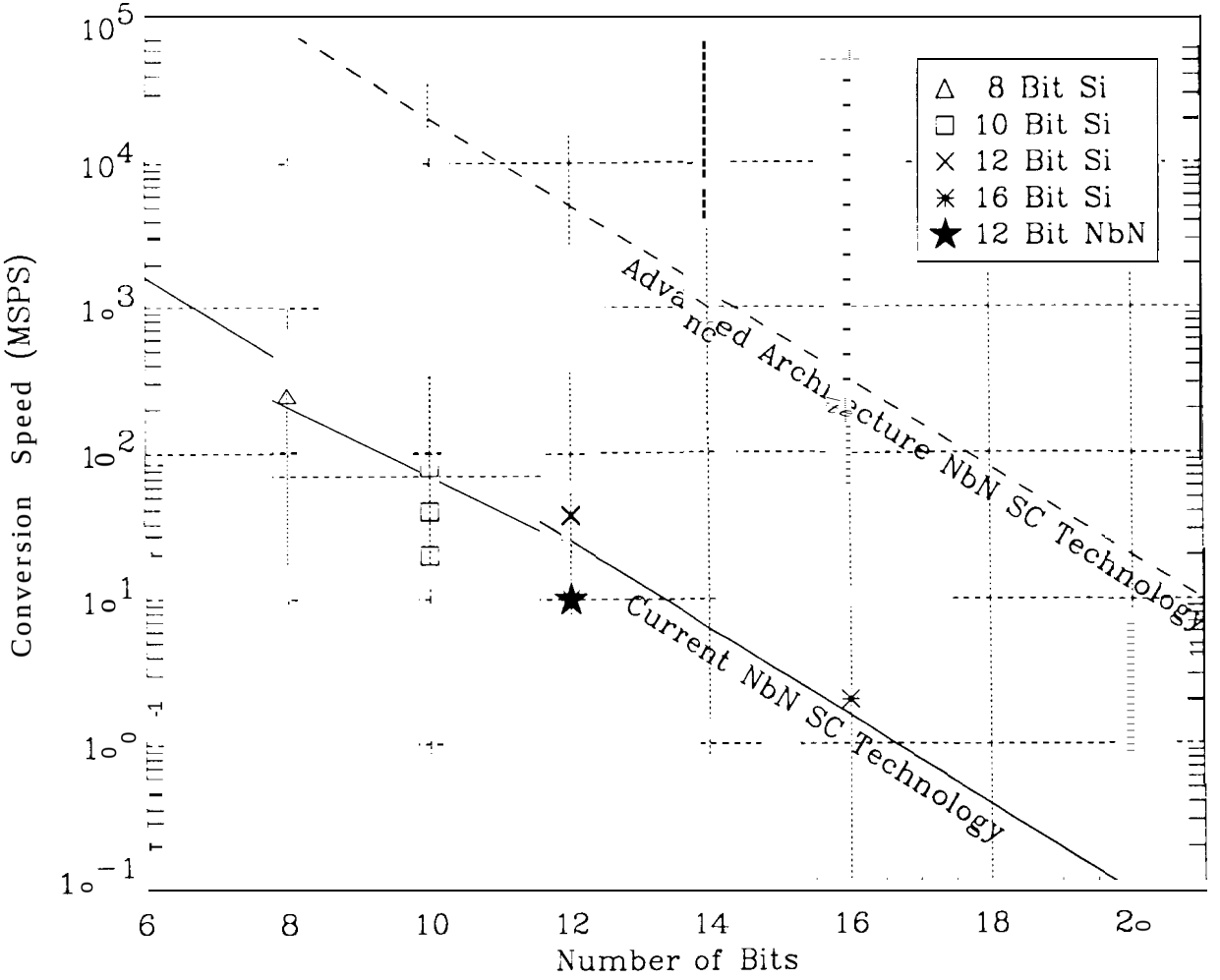
Sensor System Test Bed

The sensor system testbed activity is jointly funded by the Ballistic Missile Defense Organization, the Naval Research Laboratory, and the National Aeronautics and Space Administration/JPL.

Value of the Test Bed:

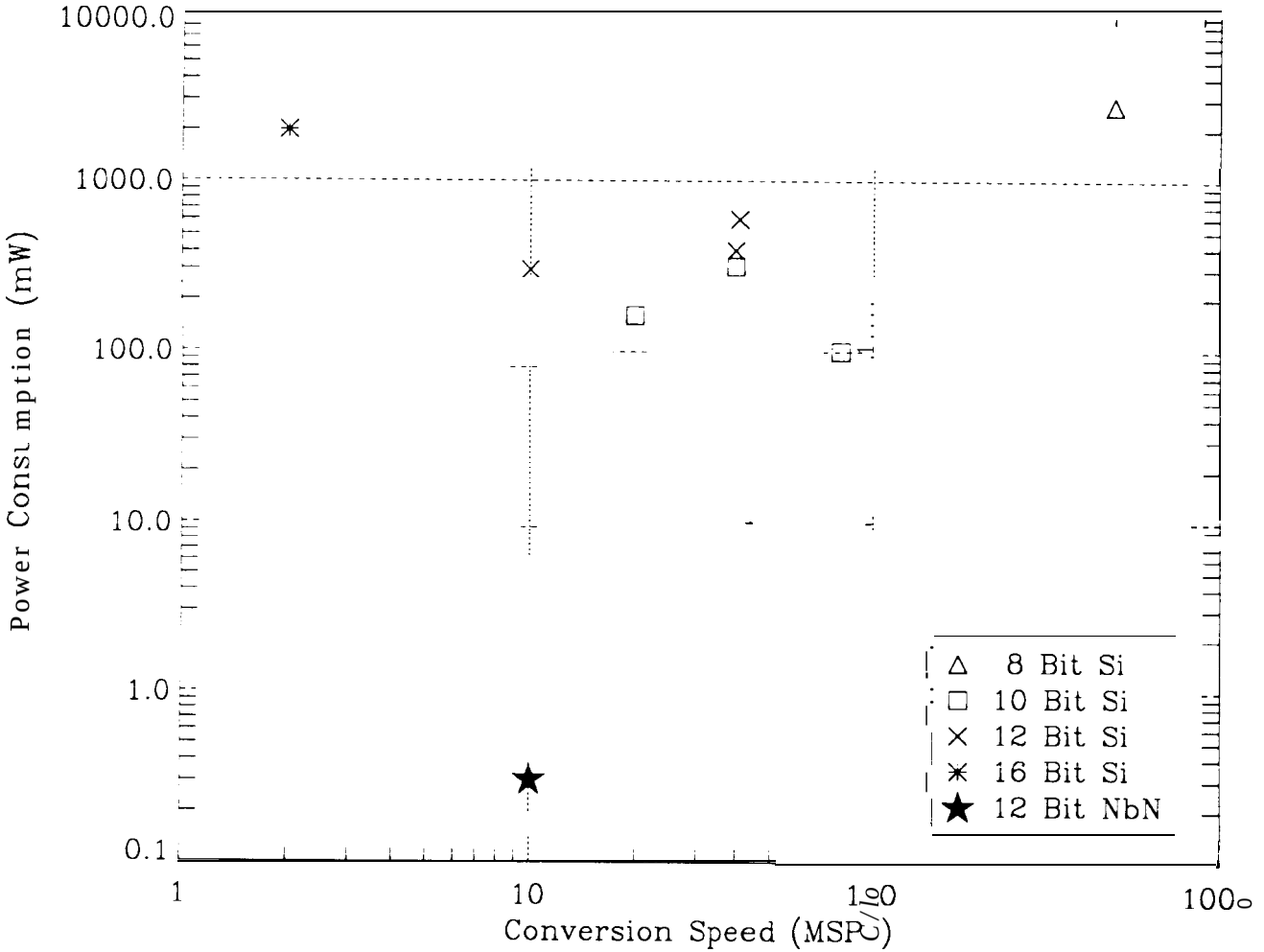
- Establishes a JPL capability for 2–30 Kelvin system-level evaluation of new instrument component technologies (*e.g.*, advanced focal plane arrays readout electronics, interface electronics and analog-to-digital converters).
- Provides an essential bridge between component technology development and instrument applications projects.
- Provides a neutral site testbed for the evaluation of advanced instrument components which are being developed by foreign and domestic suppliers.

SCE Advantages — Speed



Projected speed is more than two orders of magnitude faster than present Si technology.

SCE Advantages — Power



Power dissipation is more than two orders of magnitude lower than present Si technology.

Potential Applications of SCE

High S/N imaging for high background interceptor seekers and space surveillance optical sensors.

- VLWIR image digital signal processing on the focal plane
- Multispectral processing in real time.
- Order of magnitude reduction in system power, including refrigeration penalty

Ultra high performance computing

- >10 GHz clock speeds

High data rate, multiple access communications networks

Slow frame rate, large IR arrays - astrophysics

- multispectral camera with $\geq 512^2$ arrays
- use SCE to lower power dissipation by using one ADC and processor

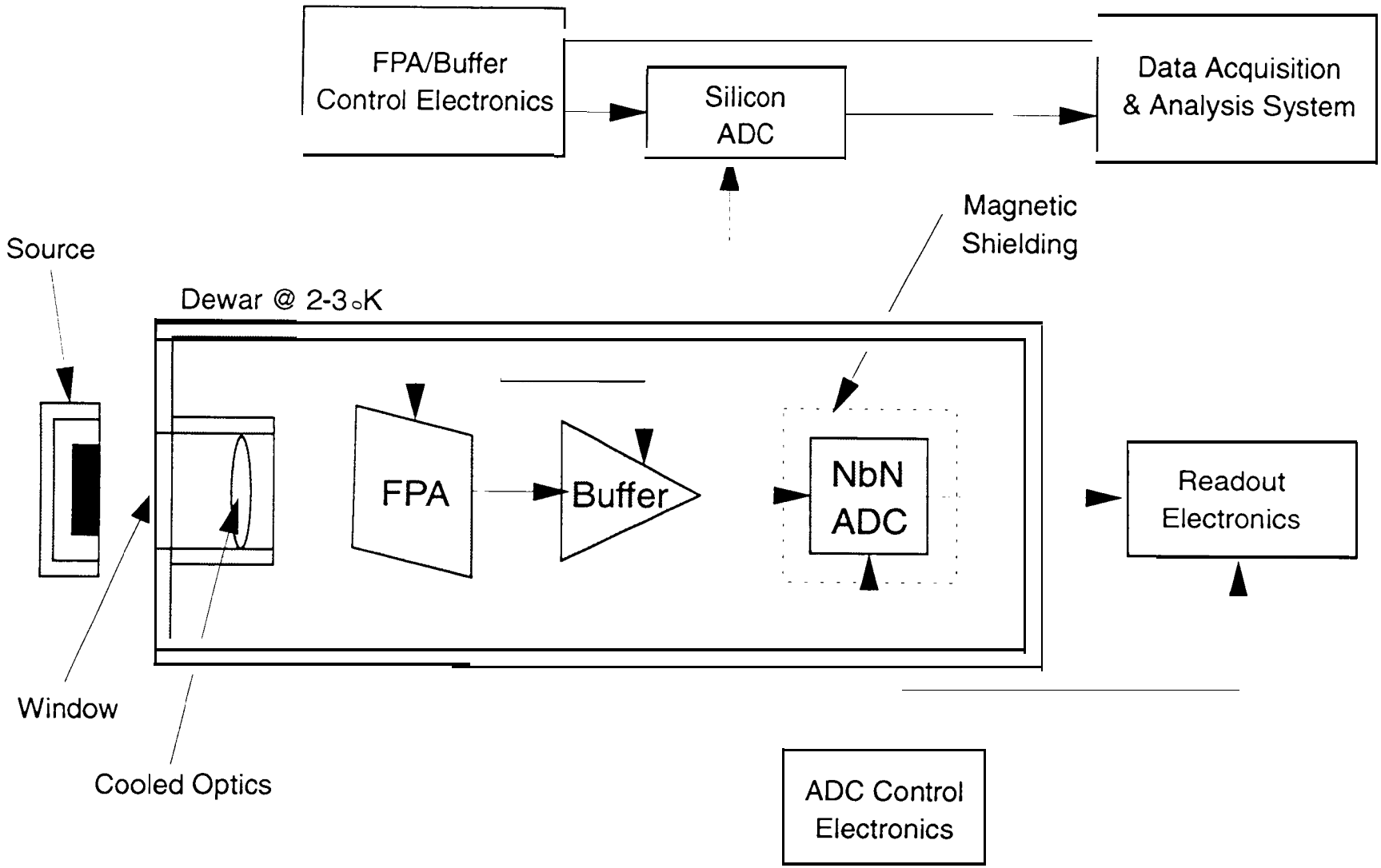
Fast frame rate large IR array, Earth atmospheric sounding

- Hyperspectral therma IR dispersive imaging spectrometer
- use SCAPCs to read out Si:As IBCs for monitoring data in 8–14 micron region

Very fast frame rate moderate IR array - Earth remote sensing

- imaging Fourier transform spectrometer
- utilize SC ADCs to achieve frame rates (>10 kHz) necessary for FTS operation, and use SC processors to do data processing

System Block Diagram



FPA Characteristics

Rockwell (now Boeing) High Flux Arsenic-Doped Silicon Blocked Impurity Band (Si:As BIB) Hybrid Focal Plane Array.

Number of Elements:	128×128
Pixel Pitch:	75 microns
Spectral Response:	2 to 28 microns
Operating Temperature:	4 to 14 K
Frame Rate (Max):	400 per second
Number of Outputs:	16
Data Rate per Output (Max):	4×10^6 pixels/sec
Output Voltage (Peak-peak):	+5 V (zero flux) to +3 V (saturation)

Buffer/Multiplexer Characteristics

Requirements:

- Multiplexes the detector's 16 voltage outputs onto a single signal line
- Provides a single voltage output for the external ADC
- Provides a single current output for the superconducting ADC

Approach:

- Fabricate the buffer as a small-scale IC using gallium arsenide junction field-effect transistors (GaAs JFETS). This fabrication technology is available in-house at JPL.

Performance:

Power Required:	1 mW
Size:	9x9 mm
Speed (Min):	100 MHz
Operating Temperature:	4-300 K
Current Output:	0-500 microamps
Voltage Output:	+8 V to +6 V
Noise:	1 microvolt/sqrt(Hz) at 4 K

Data System

Data System Requirements:

- Control and operate the FPA, buffer, and both the Si and NbN ADCs in a synchronous manner
- Allow a direct interface with Si and NbN ADC inputs
- Accept data at 10 MSPS (170 MHz serial bursts)
- Store images on disk for future processing
- Display selected frames in real time
- Analyze stored data for missing codes, linearity, noise, etc.
- Compare Si and NbN ADC performance

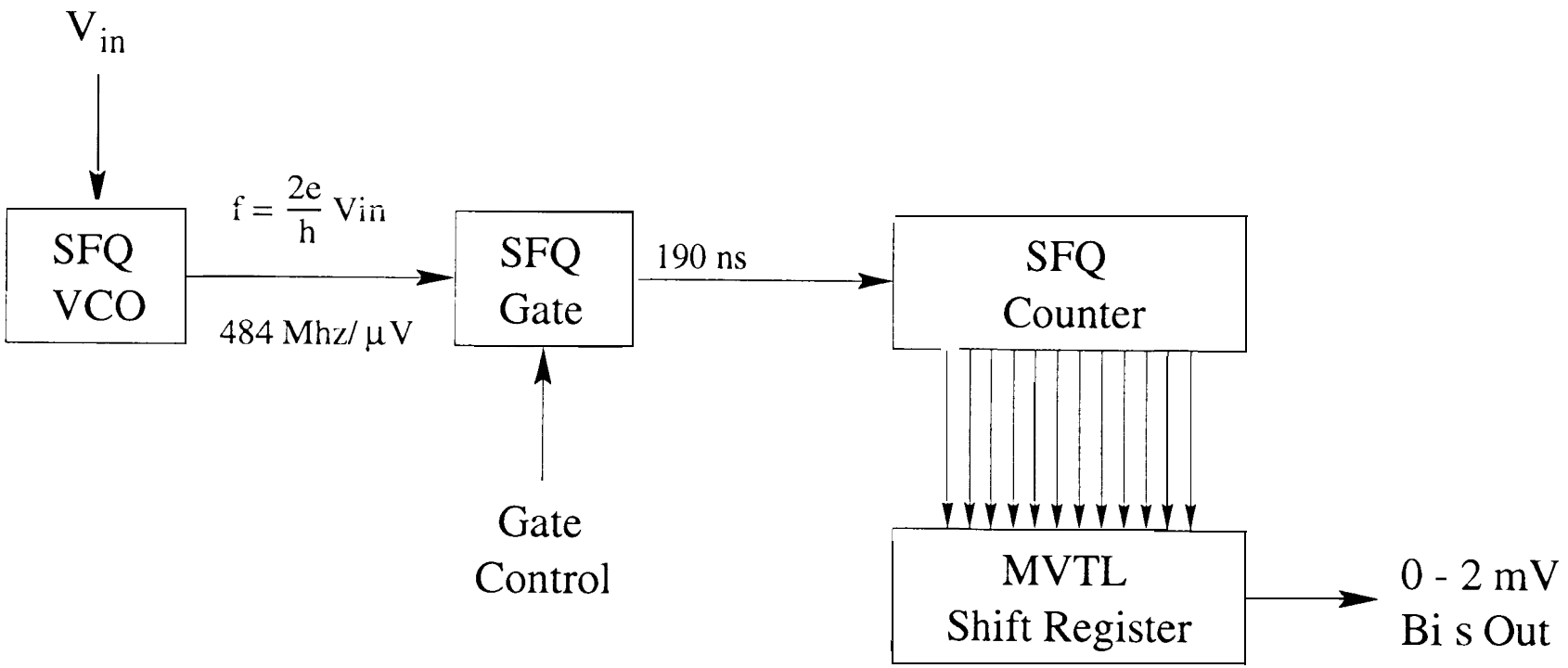
Approach:

- Use available control equipment where possible
- Fabricate interface box to convert NbN ADC output signals to levels acceptable by data acquisition computer (RF amp and ECL logic)
- Interface box operates at room temperature
- Data acquisition computer is a fast PC with ultra-wide SCSI disk interface

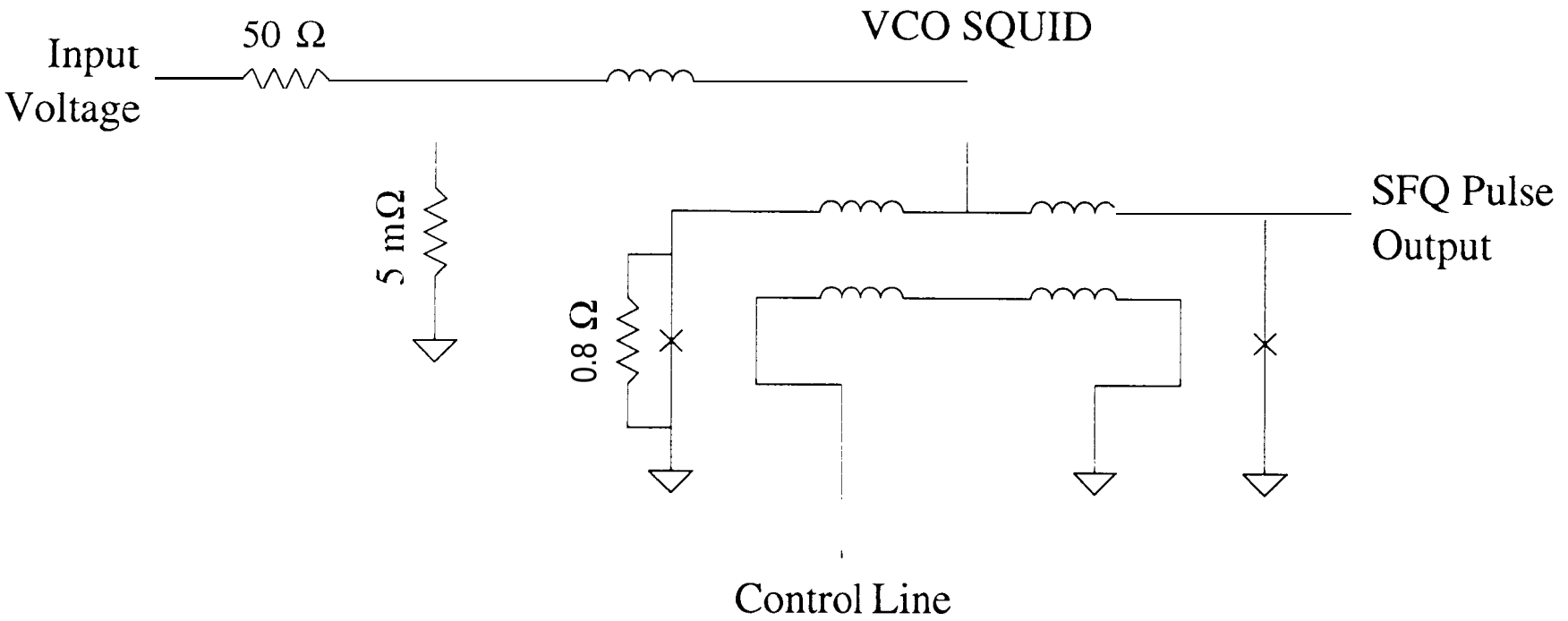
A/D Converter Overview

- Supplied to test bed by TRW
- Based on niobium nitride Josephson junction technology
- Operates at a temperature of 10 K
- Processes data at 10 MSPS with 2-bit conversion
- Input is 0–150 millivolts, single-ended
- Outputs are a sing e serial data line, bit clock and word clock provided by control electronics
- Output evels are 0–2 mV into 50 Ohms.

ADC Block Diagram



Input Characteristics



I–V relation for the 5 mΩ shunt resistor in combinat on with the VCO SQUID is (slightly) nonlinear, thus:

$$Count = T_{gate} \frac{2e}{h} I_C \, 5\,m\Omega \sqrt{\left(\frac{V_{in}/50\Omega}{I_C}\right)^2 - 1}$$

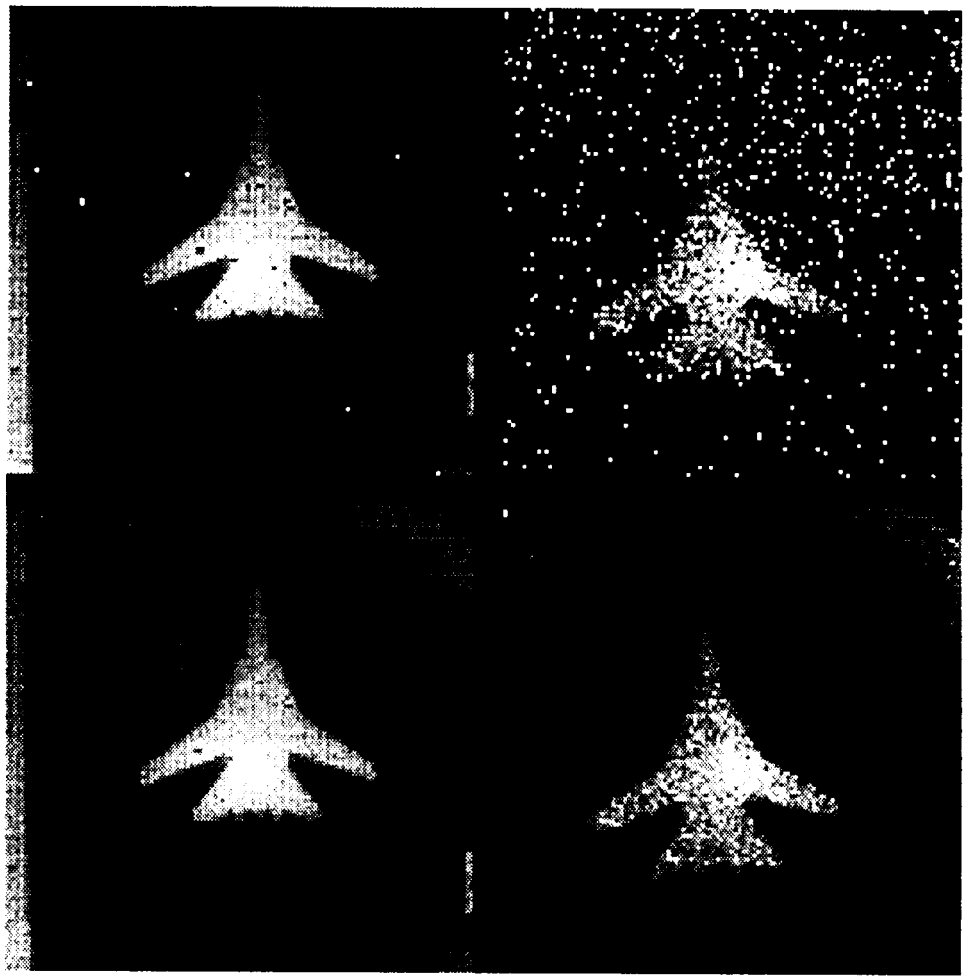
Results

A superconducting digital integrated circuit has been used as a component in a "real-world" system for the first time!

Images

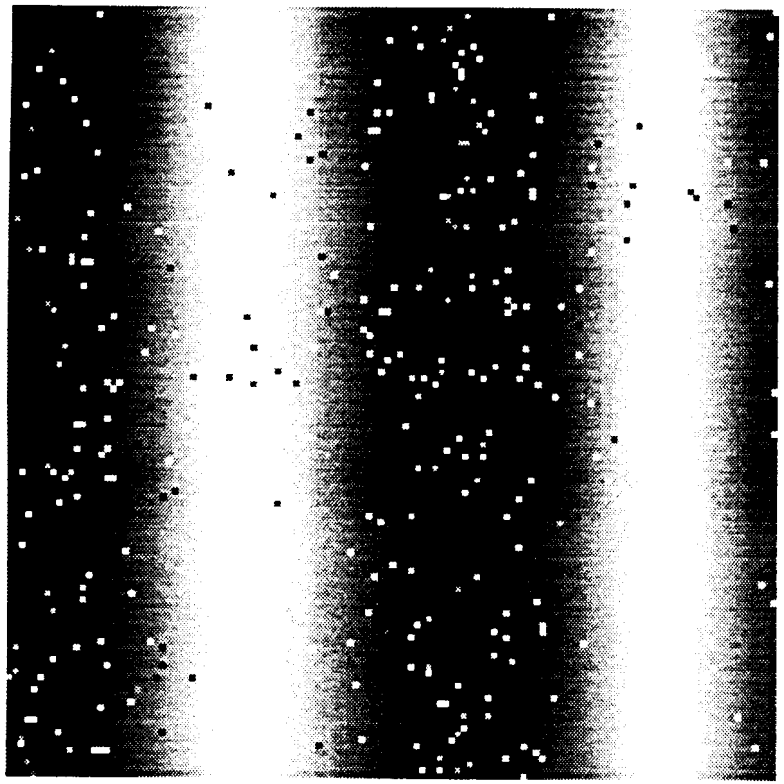
Images of various objects in the lab (clockwise from top left): fingers letters and soldering iron, toy airplane, letters through a silicon wafer.

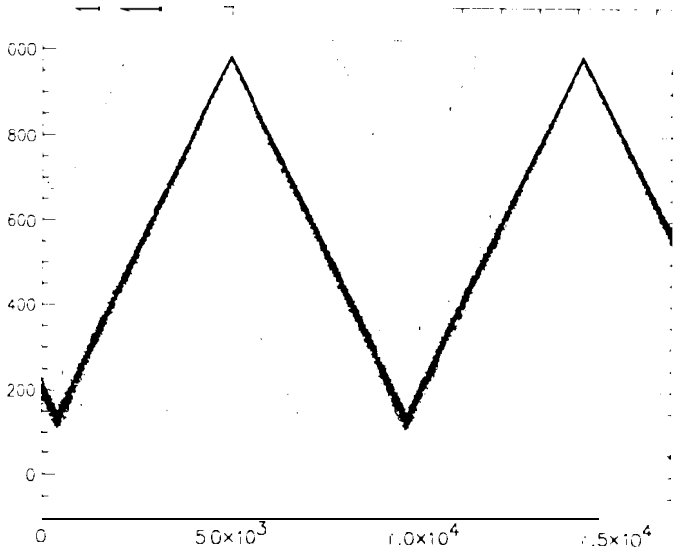
Comparison images with Si ADC



Comparison images show that while noisier, the NbN converter images have the same essential features seen in the Si converter images.

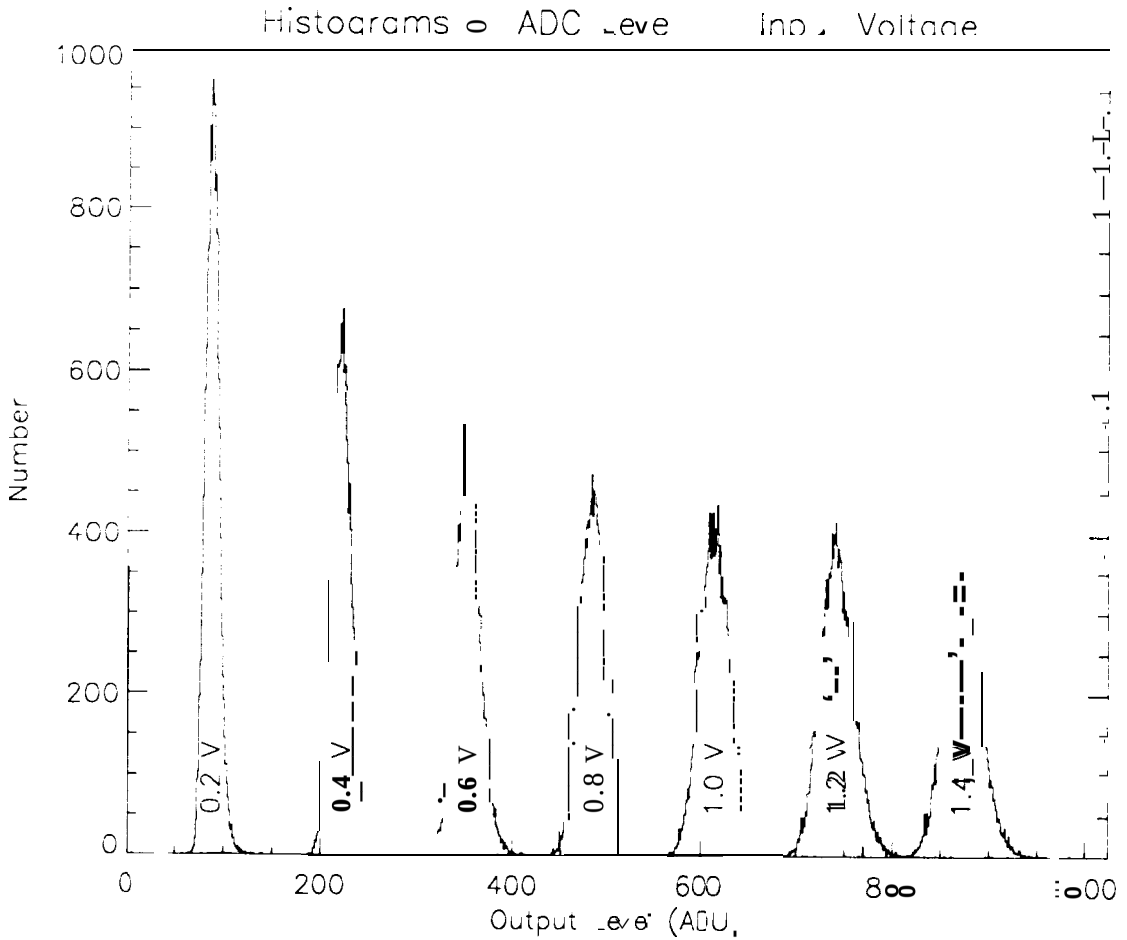
Ramp/sine images





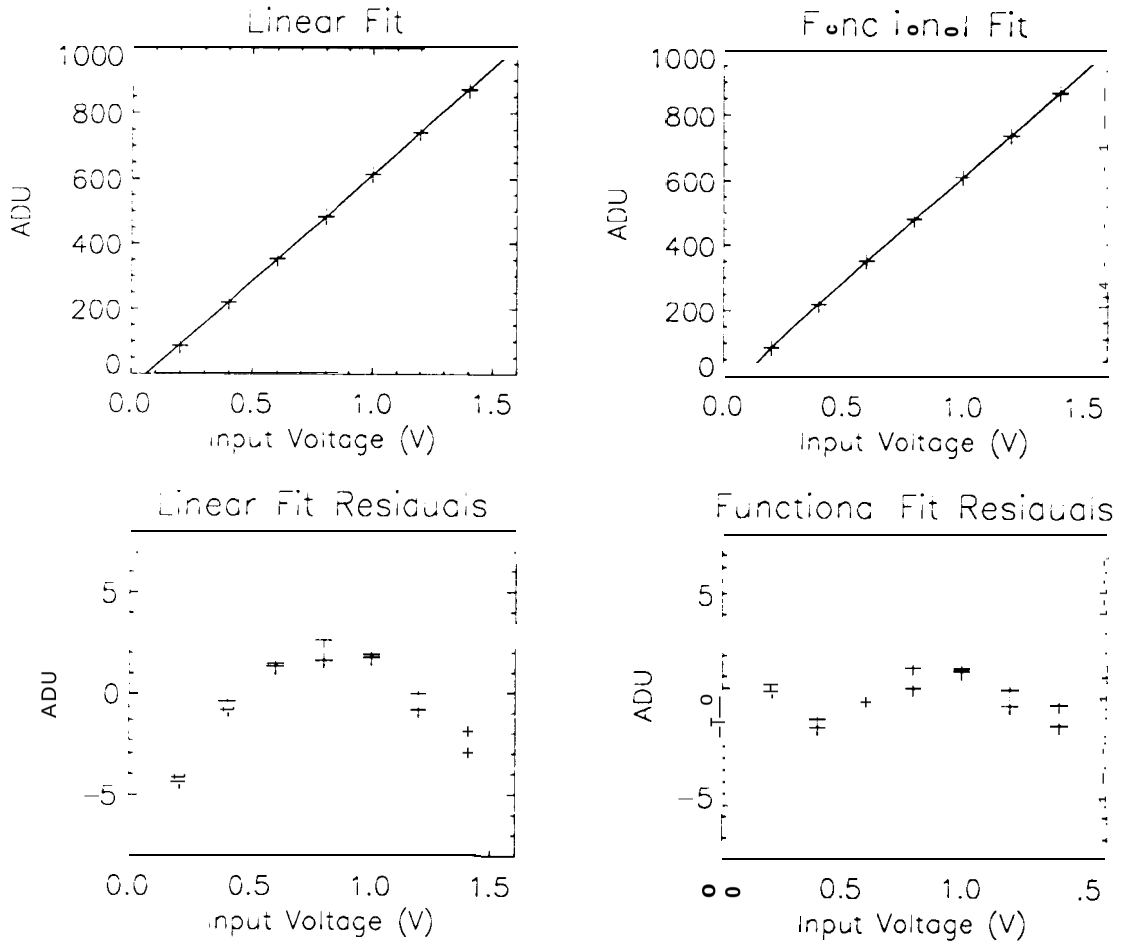
Typical "image" of a function generator input. Bit errors (full scale and single bit) are seen in the plot.

Levels



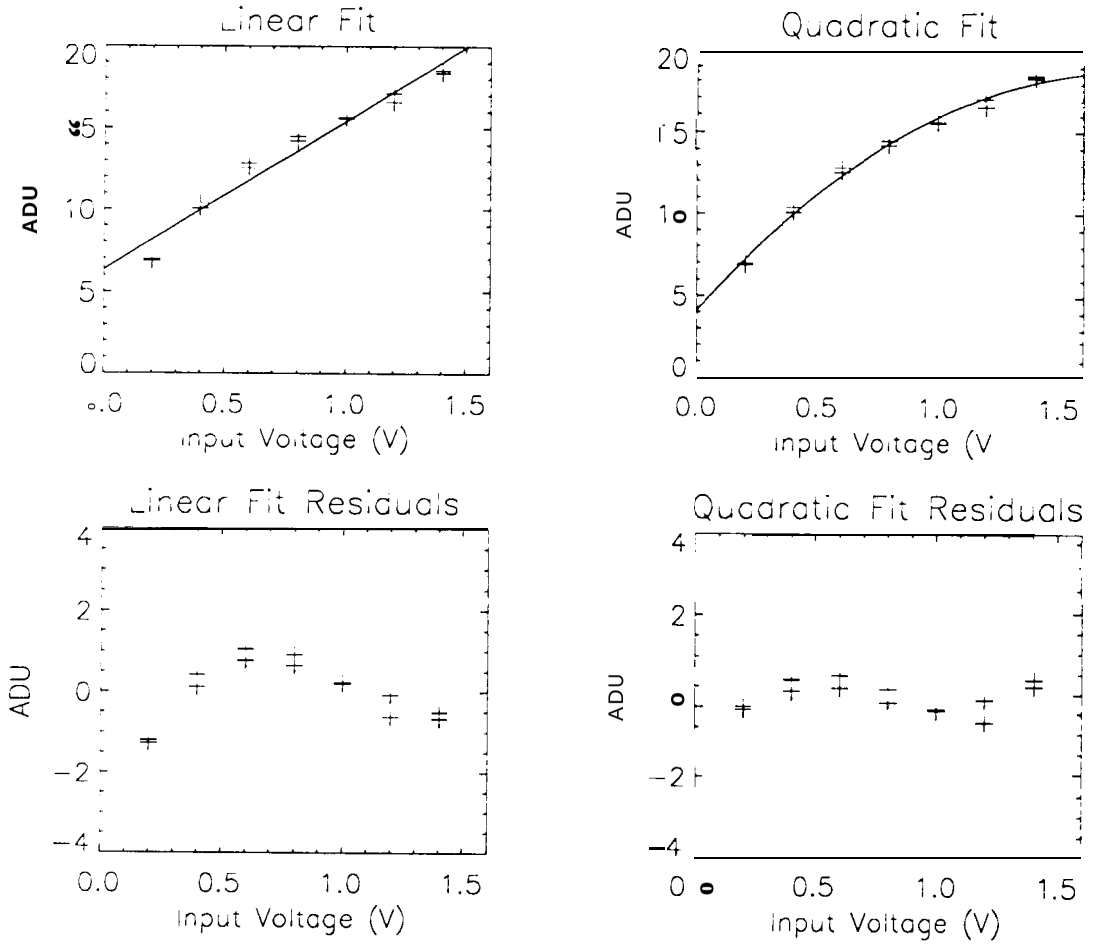
Histograms showing measurements at 7 DC voltage input values.

Linearity



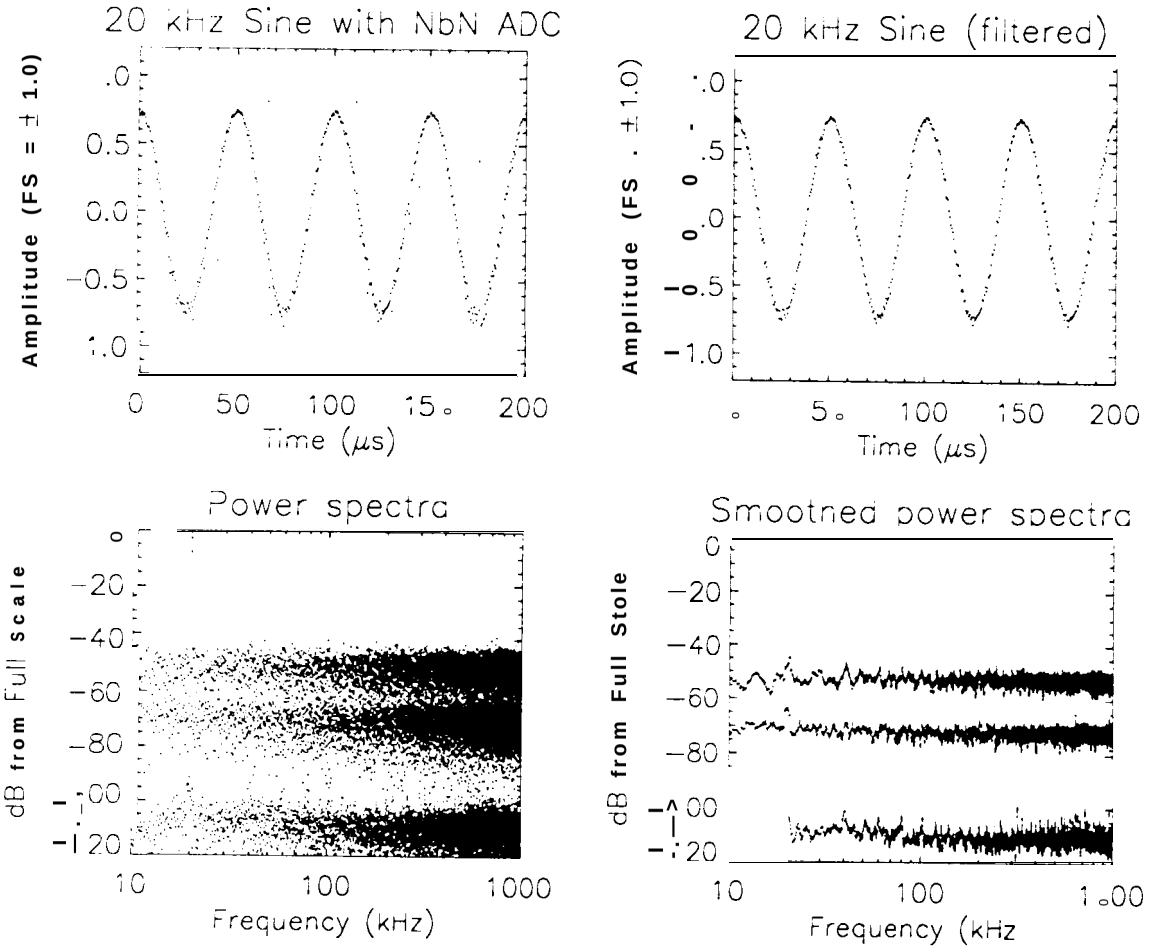
Plots showing the linearity of the converter. The left column is a simple linear fit to the data; the right is a fit using the theoretical I–V relation for a shunted SQUID oscillator.

Noise



Plots of the noise as a function of the input voltage. The source of this excess noise is not yet understood.

Spectral Characteristics



Power spectra for both the NbN and Si converters.

...ture ADC work

Near-term work:

- System size reduction
- Incorporation of improved TRW ADC
- Incorporation of TRW DSP chips (background subtraction and gain correction)

Possible longer term:

- Evaluation of Hypres 16-bit Nb ADC
- Rapid cool-down capability
- Add superconducting memory to TRW DSPs
- Flight demonstration

High T_c possibilities

- Architecture is directly transferable
- Current roadblock is simply how to make chips with high-T_c materials

Conclusion

Under sponsorship of BMDO, NRL, and NASA, JPL has established a testbed capability for 2–30 K system-level evaluation of new instrument component technologies.

The TRW superconducting analog-to-digital converter has been integrated with semiconductor components and successfully demonstrated in an infrared instrument system at 10 Kelvin.

The instrument system testbed is available as a neutral site for evaluation of advanced instrument components.