DEVICE SEE SUSCEPTIBILITY FROM HEAVY IONS (1995-1996)

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Abstract

A seventh set of heavy ion single event effects (SEE) test data have been collected since the last IEEE publications. SEE trends are indicated for several functional classes of ICs.

Introduction

SEE test programs at JPL, The Aerospace Corporation, and other organizations are continuing, in order to assess specific part performance and trends. Six compendia have been published since 1985-- in IEEE-NS Transactions (1 ,2,3,4) and the Workshop Record (5, 6). In this paper, the authors extend the data base for 240 new parts, arranged according to technology, function and manufacturer in order to identify trends and data gaps.

The compilation of data are presented in tables very similar to those of previous compendia. However, a separate column is now provided to highlight latchup response, by listing the latchup LET threshold in units of MeV/(mg/cm^2) and the device latchup cross section. The listed cross section is not always tied so closely to a fixed beam ion LET as that for soft errors. Thus it should be regarded as only representative. In earlier papers, these data were listed in the "Remarks" column when known.

It should be emphasized that these data are new. For a complete compendium of all existing SEE data, one needs to use this paper in conjunction with references 1 through 6. Older data are, of course, less likely to describe present day device response-- even those taken for the same manufacturer and number. The best data is that taken for devices of the same well-defined lot; a rarity in this era of widespread use of commercial devices.

Testing Approaches

The experimental procedures, such as those used by JPL and The Aerospace Corporation, are evolutionary and are described in detail from time to time in December issues of IEEE Transactions on Nuclear Science (7,8) or in in-

house reports. In general, procedures comply with the updated guideline for SEE testing set forth by the ASTM F1.11 document (9).

Organization and Scope of Data

This paper summarizes soft error and latchup experimental test data of 1995 and 1996 from the Jet Propulsion Laboratory (JPL), The Aerospace Corporation (A), the Goddard Space Flight Center (GDD), and others. Not included are data sets on power transistor burnout and single event gate rupture reported by JPL in 1994 (10) and updated in1996 (1 1), which require a more complicated format, The most recent 1997 data is also not here-- see instead JPL's RADATA data base (16).

The 1995-1996 data and some early 1997 data are presented in Table 1. These data represent a substantial abbreviation and ignore statistical features altogether. Users are cautioned that manufacturers (See Appendix I for manufacturer abbreviations) may often change their process and thus device SEE susceptibility, without changing part number or notifying outsiders. Hence, a confirmatory test of flight parts is always good policy. Additional appendices supporting Table 1 are Appendix II, Abbreviation of test organizations, and Appendix III, Abbreviation of test facilities. Appendix IV is a copy of a data page that was inadvertently omitted from the corresponding table of the 1995 compendium (6).

Trends & Limitations

Trends and device comparisons in the recent data are offered in the "Remarks" column of Table 1 and in the following section. The organized tabular format is designed to facilitate comparisons. Special studies, such as the nature of single event transients, variation of SEE response with temperature, or a comparison between heavy ion data from different test facilities, are beyond the scope of this presentation.

An Evaluation of SEE Data

All data are broken down according to certain functional categories for ease of reference and convenience in comparison. These categories include microprocessors & microcontrollers, logic devices, RAMS, PROMS, ASICs, gate arrays, A/D and D/A converters, DC/DC power converters, linear devices and miscellaneous devices,. In addition there are new data categories or subcategories for ECL bipolar logic, CMOS DSP'S, flash memories and Ethernet (LAN) devices.

Test temperatures are at ambient unless otherwise noted. It is well known that higher temperatures exacerbate latchup phenomena and often so do higher voltages. Thus JPL and others may impose these conditions [within spec] on the test. Lot date codes are provided when they are known and are meaningful. Commercial date codes may bear little relation to lot fabrication-- they may refer instead only to receipt or delivery of parts batches.

References to threshold mean that a measurement taken with a fluence (time-integrated flux) of 106 ions/cm^2 yielded no upsets (soft errors or latchup)

unless otherwise noted. The LET is the “effective LET “ obtained by multiplying the inherent beam LET (dictated by the ion species and its energy) by the secant of the incident beam angle as measured from the perpendicular.

The concept of effective LET, that it is proportional to deposited charge in a wafer-like sensitive volume of large lateral dimensions, is often appropriate but frequently challenged. It does not usually apply to permanent errors nor very small elements, such as DRAM cells. Also data obtained by two different ion species having the same effective LET never match exactly, as is to be expected,

The end usage of SEE data is often a calculation of SEE rates for a known environment. For such calculations, a plot of device cross section vs LET is highly desirable and may require a computer to integrate the flux over LET and incident angle, for some assumption regarding the shape of the sensitive volume. It will be necessary to refer to the literature in IEEE Transactions on Nuclear Science (December issues) to pursue this calculation.

As a last resort, a very coarse approximation that will always overestimate the true rate is obtained by multiplying a step function approximation for the cross section (say, its saturated value above the threshold LET) by the “effective flux” of ions (including obliquely incident ions) having an “effective LET” equal to or greater than the device’s measured threshold LET. If the rate calculated in this approximate manner is acceptable to the user, the more exact calculation may not be necessary.

A. Microprocessors & Microcontrollers

Several test groups obtained SEE data for microprocessors this year, and the emphasis remained on investigation of 32-bit machines. However, Matra Harris Semiconducteurs listed a set of five 8-bit Temic type microprocessors in their “Temic/Matra MHS Radiation Evaluation Results Table” (July, 1996). A high latchup resistance was an important common denominator for the Temic machines.

Latchup data for 32-bit microprocessors included IDT's CEMOS-5 technology, with a latchup threshold that varies with choice of epi thickness. Also tested were Intel’s 386 and several variants of the 486 machines; the CHMOS IV technology is susceptible to latchup, but the later CHMOS V (0.8 micron feature size) variation showed higher resistance to latchup. Conspicuously missing are test data for any of **Intel’s Pentium devices,** but a JPL test [unpublished] of the AMD Pentium showed it had a very high latchup sensitivity to heavy ions and protons. CNES (France) tested the INMOS T805 transputer extensively and evaluated dynamic vs static test modes, with cache enabled or disabled. The transputer had a modest latchup threshold [See Table 1.] IBM (now Lockheed Martin Federal Systems) tested one of five chips comprising Loral's RAD6000 machine, fabricated with RHCMOS-E technology. These data showed a relatively high soft error threshold and the only demonstrated immunity to latchup of the 32-bit machines during this test period. Note, however, that other latchup-proof machines may exist, such as the 32-bit Mongoose reported in an earlier compendium.

Soft error thresholds are consistently low to moderate for these machines, with LET threshold [LET(th)] ranging from <2 to 15 MeV/(mg/cm^2). Most of

these microprocessors were also very susceptible to latchup as noted. Aeropsace provided a set of data for Motorola machines, having low soft error and latchup thresholds. The hardest part tested in this period was the Loral chip. It and some other evolutionary versions in development offer a tempting new addition to the limited set of tested rad hard, high-capability microprocessors.

Testing of several microcontrollers and various other processors included 8-bit, 16-bit and 32-bit machines. All of these devices were susceptible to soft errors and latchup, with the exception of the very hard Plessey 2901 microprocessor slice.

We are still waiting for the arrival of radiation-hardened DSP's. Note that DSP's latchup readily, and one 32-bit DSP (TIX SMJ320C30GB) exhibited snapback at a low LET.

B. Logic Devices

The era of massive testing of logic devices seems to be over. There are some new data for 3V devices and for ECL (bipolar) technology for the first time. The ECL technology provides high-powered but very fast (<1ns) devices. There are also data for phase lock loops; the latter devices demonstrate frequency shifts and other types of lost functionality.

C. Static Random Access Memories (SRAMs)

There is little SRAM data this period. The largest bulk of SRAM data were taken from a table presented by Matra (Temic) at a recent IEEE conference, and little is known about test details. It appears that all these CMOS devices are consistently resistant to latchup.

Again we see Aerospace tests of ECL technology -- latchup-proof as expected. ECL tests include low capacity SRAMS with a heightened SEU vulnerability relative to their CMOS counterparts. Their high power requirements imply that external temperature control be provided. This problem, and the need to adjust logical levels to CMOS voltages have inhibited testing of ECL in the past.

D. Dynamic Random Access Memories (DRAMs)

A block of data for 16 M DRAMs taken by LaBel [12] yield some interesting generalizations. As always, DRAMs have a very low LET threshold (usually <1.4 MeV/mg/cm^2) and very high cross sections (up to 3 cm^2.) Most errors are standard single bit upsets (SE US) or latchup (SEL). Block errors sometimes occur, however, in which a single ion strike causes a (partial or full address) column or row to be in error. Also observed was a single event functional interrupt (SEFI)-- a test or standby (low power) mode of operation with original currents, requiring either a reinitialization or a power cycling to recover. More detailed studies revealed that the SEFI failure mode will not occur if normal refresh rates are maintained.

Stuck bits which cannot be reprogrammed after irradiation were also sometimes seen. The stuck bits can be handled by an EDAC code in a manner similar to single bit errors as long as they do not occur with high frequency. The

EDAC code would simply detect them and correct them. Multiple bit upsets (MBU) in which a single ion strike induced multiple upsets within a word or byte are not observed nor expected. This problem is prevented by the physical design layouts in which physically adjacent cells within the device (which might upset simultaneously) belong to different logical words.

His test results also showed little dependence on the test mode (dynamic or static) nor access method (byte or page.) This is consistent with the fact that refreshing of memory cells is typically going on when the device is not being written or read. Thus, even in a static (data storage) mode, cell access through memory refresh cycles is being performed.

One data entry (Toshiba TC51 832p DRAM) was reported for the "quasi-heavy ions" provided by a He-ion microprobe, T. Matsukawa et al [13] have used a microprobe at Waseda University, Tokyo, to focus one or more 1.0 to 4.5 MeV He ions onto a 2 micron diameter area. By counting the ions, delivered in **5** microsec intervals, they can determine an equivalent LET threshold for their test device. One limitation of this technique is that it is "only applicable to devices with a sufficiently large time constant of its circuitry, " such as DRAMs and nMOS SRAMS. Ion doses were found to be insignificant,

E. Flash Memories & PROMS

A new device category was opened for flash memories, in response to several recent tests. A flash memory is an EEPROM plus microcontroller or state machine located on the same chip. These devices are of high present interest because they provide a useful alternative to high-density commercial storage technology not requiring frequent write operations. Tests by JPL [14] and ESA [15] are especially noteworthy.

l-he JPL test explores in depth the Intel SV (smart voltage) and Intel -SA versions of a 16 Mbit flash memory as well as 16 Mbit & 32 Mbit Samsung flash memories. The dominant responses are control errors induced by the microcontroller (or state machine.) This is evidenced by some test runs in which the control regions of the flash memory are masked out In one instance, such a shielding permitted individual memory soft errors to become visible-- for the Intel SV version, with a well-defined threshold and cross section. However, it is the control errors that provide the greatest interest. They are fairly rare (see cross section and LET threshold data in the table or Ref. 14), but they are devastating. Failure modes include many lockups, requiring power-down and restart to continue test. Failures can arise from stuck bits (SAM 16 Mbit only), high current modes (205 mA) released during the read mode, partial byte flips, whole device flips, temporary high current spikes (tens of mA.) Tests were performed during "read mode" (read only after irradiation of the static part) and "write mode" (erase, write & read during irradiation.) The effects were worse during "write mode, " and frequently included block erasures. However, the latter scenario is expected to be rarely used in space. Test were also performed on unpowered devices to confirm that the memory contents were safe in that mode.

The ESA test surveyed many different kinds of volatile memories including several older and smaller (-1 M) flash memories. It included data for three main groups of devices: namely, Ultra Violet erasable Electrically Programmable Read Only Memories (UVEPROMs), Flash-Erasable and Programmable Read Only

Memories (flash EPROMs also known as flash memories), and Electrically Erasable and Programmable Read Only Memories (EEPROMs.) Some of the data in Ref. 15 were published in the previous JPL compendium [6], so not all were included herein.

ESA'S UVEPROMS and flash memories were programmed prior to test and only checked in the read mode. The EEPROMs were programmed during the test and measured in both read and write modes. For SEE testing in the read mode, following programming, normal read cycles were carried out to check the memory content. In the write mode, a test cycle was used-- first a write "1" followed by three read cycles; then a write "O" followed by three read cycles. The three read cycles allow the separation of errors into "read errors" having one error in one of the three read cycles and "write errors" having the same error in all three cycles. None of the three groups of parts exhibited any type of SEE. when they were unbiased.

ESA data included measurements for transients, soft errors and latchup. Transient errors occur in some parts from all three groups; they are a corruption of the read cycle. Transients in the UVEPROMs cause no loss of memory content, but the content may or may not be lost in flash memories. Flash memories exhibit other peculiar effects, such as single bit errors, word errors, 1K page errors and complete erasure. However, none of the flash types showed latchup, transient errors or SEUS during proton testing of> 1010300 MeV protons/cm^2. EEPROMS showed more errors when tested in the write mode than in the read mode. However, read mode tests include such error modes as transient bit, word and block errors; "chessboard" address errors; latchup and device erasures. Write mode tests showed errors or loss of functionality, latchups; bit, byte and block errors; address failures at higher LETs. Write tests with protons also show errors in some EEPROMS.

F. Application Specific ICs (ASICs), Programmable Array Logic (PALs) & Field Programmable Gate Arrays (FPGAs)

Flight applications of FPGAs are increasing as more designers start to utilize these devices. In the commercial and military market places, devices with new architectures and increasing performance and density levels are constantly appearing. A variety of NASA, ESA, and industry groups are involved in the testing and evaluation of these devices.

A strong experimental and tutorial effort was provided by R. Katz (17) who warns that interpretation of FPGA data and test configurations is non-trivial. For SRAM-based FPGA's, he notes that along with typical data upsets, the configuration of the part may be changed by an SEU in the configuration cell-- dubbed Single Event Reconfiguration (SER). Other classes of errors include upsetting on-chip reset circuits in an FPGA, an effect seen earlier in a PAL or a TAP controller. Katz also warns that Actel dice are fabricated by more than one foundry, implying again that one must take care in the use of radiation data,

A discussion in Ref. 17 also considers the unintentional reprogramming in flight of any programmable device. Failure modes are seen when open fuses become reconnected over time He notes that many of the new programmable logic technologies are susceptible. Examples are permanent damage to EEPROMS during a write cycle when high voltage is present; a second is the

upsets of temporary storage registers when an operation is taking place. For dielectric antifuse devices, permanent damage can occur in the antifuse programming element via many different failure modes.

G. Other Linear Devices

This category includes transceivers, drivers, receivers, pulse width modulators (PWMS), operational amplifiers and comparators. Some other linear devices are located in an earlier category for “Logic etc. ” The devices here are more complicated, and the op amps and comparators are susceptible to single event transients (SETS) -- a potentially serious failure mode which can affect nearby components.

A new subset of linear data was provided by JPL’s large scale test of six manufacturers’ RS485 transceivers, which can sometimes be used for RS422 applications. All were tested for latchup only, and several were tested at both room temperature and a worst case elevated temperature. Most of these devices were very resistant to latchup.

The op amps and some slow comparators were tested by JPL during this period (1 **8).** JPL used a technique of repeated photographic images of transients induced by several ion strikes during a run. Thus, the data showed expected variations arising from random hit locations which in turn proved to be predictive of the changes in transient response vs. LET (found later with different ions.) Their data showed serious vital signs for output transients: a low LET threshold, high cross sections, very high voltage transient amplitudes (often rail-to-rail) and extended pulse durations (microsecs.) It is expected that SETS at the output of comparators are especially dangerous, because they bridge the analog-digital interface. Some data taken for small hybrids (not reported here), such as a DCDC converter and an optocoupler, show a very drastic response to the SETS generated by a susceptible comparator within their circuitry.

H. Analog to Digital Converters (ADCs) &. Digital to Analog Converters (DACs)

A rather random selection of ADC and DAC data are presented this year. Perhaps the key question is how to interpret it. Turf linger has observed (19) that it may be correct to divide the cross section by the sample rate (for those devices which allow a variable sample rate.) The argument goes (1 believe) that single events only occur during certain portions of each clocked cycle. The more cycles per second, the more chances of upset. It is possible that this problem can be solved analytically-- at least in principle. Perhaps there are certain limits on sampling speed for which it applies. JPL was interested in testing this out, but so far have only been able to obtain test funds for a few devices with fixed internal clocks.

1. DC/D_C Power Converters

Devices of this new test category have recently received attention for space flight. A key characteristic of this device type is a propensity to lose or drop out voltage [also known as restart errors] as a result of single ion strikes. Earlier test data showed a spontaneous recovery after several milliseconds, but

more recent data have shown cases where the voltage dropout is permanent. The permanent dropout to O volts can be restored by powering off and then turning the device back on.

J. Network Interface Controllers & Miscellaneous Devices

Another new device subcategory was opened to report MMS tests of Ethernet LAN components. The data include latchup tests (which ruled out further soft error testing of some devices), heavy ion soft error tests of the DP8392 and AMD AM79C98 device, plus some proton test data. The existence of proton soft error upsets for NSC's DP83932, DP83956 [which were untested for heavy ion soft errors] can be used to infer a heavy ion cross section threshold of <10 MeV/mg/cm^2. The soft error cross section for the bipolar DP8392CV coaxial transceiver interface device was characterized extensively, since it did not latchup. Different susceptibilities are reported for the “transmit mode” and the “receive mode. ” The data is presented as cross section per transmitted bit, in keeping with other types of electrical characterizations.

Conclusion

As always, it is important to realize that test data may not be applicable to the devices a project has in hand, due to known or unheralded changes in fabrication. This observation is especially likely to be true if the device type is in the forefront of recent developmental or evolutionary changes. Where known, such differences in fabrication are listed in the table, but there has not been a concerted effort to provide this information consistently by all test groups. Such lack of information is also a price one pays for using commercial off the shelf parts (COTS), The best insurance of system protection is an accelerator test of flight parts from a well-defined flight lot.

Table

Table 1, SEE Datafor 1995-19%

Test	Org	Device	Function	Technology	Mfr	Tested Bits	Effective LET Threshold MeV/(mg/cm2)	SEU Cross Section (cm2)	Device SEU cross Section Per Bit [sq micron]	Facility	Latchup (LU) Data--- L E T threshold device cross section MeV/(mg/cm2) & cm2	Remarks &
Microprocessors												
		11 E (Temic)	MicroP(8-bit)	CMOS	MTA	5	—		50	Unknown	No LU>75	TEM
		12E (Temic)	MicroP(8-bit)	CMOS	MTA		—		40		No LU>100	TEM
3	TAM	80486DX4	MicroP (32-bit)	3LM CMOS [3.45V] 0.5 mic	AMD	various	~1.5 [cache enabled]	2.5E-3 @ LET=25 [unsat]		TAM	LU(th)=~5	Eight error modes seen. Kouba & Choi, Test Report Dec. 30, 1996
							~4.5 [cache disabled]	2.5E-3 @ LET=25 [unsat]				Same as above.
3	NRL	79R3081 RISC	MicroP (32-bit)	CEMOS-5 (6,8,10,12 mic epi)	IDT	—	—	—	—	BNL	LU(th)=12;4E-3cm2.	LU data listed for 12 mic epi. For 10,8,6 mic epi, LU(th) = <26,~30, >60. Stapor, RADECS95
3	GDD	80386DX,20&25	MicroP (32-bit)	CHMOS IV	INT	—	2,4	1E-4 to 1E-3	—	BNL	LU(th)=29;1E-4 cm2	Nondestructive LU. Moran, RADECS95 p.263
3	GDD	MQ80386-25/B	MicroP (32-bit)	CHMOS IV	INT	Custom S/W	4.5 (lockup cleared by reset)	5.5 (cleared by power cycle)		BNL	LU(th)=31	Microlatchup only. LaBel, 96 IEEE Workshop Record
3	GDD	MQ82380-25/B	Integral peripheral	CHMOS III	INT	Tied to 386.	3.4 (reset errors cleared by reset)	---		BNL	LU(th)=15 to 20	Microlatchup. A classic LU or SEU self-test? LaBel, 96 IEEE Workshop Record
3	GDD	80486DX-33	MicroP (32-bit)	CHMOS IV- 1.0 mic.	INT	Syst. routine	~3 [cache enabled]	2E-4	---	BNL	LU(th)=20.	LU is catastrophic. Moran, LaBel et al, RADECS95 p.263. See below
3	GDD	80466A-21	MicroP	CHMOS IV (repackaged)	SPE	Custom S/W	5.5 (count), ~4(lockup cleared by reset)	6 to 11 (lockup		BNL	LU(th)= ~36	Microlatchup only. LaBel, 96 IEEE Workshop Record
							cleared by power cycle.)	~5 [cache disabled]	~5E-5			Same as above. Proton data exist
3	GDD	80486DX2-66	MicroP (32-bit)	CHMOS V- 0.8 mic.	INT	Syst. routine	~5 [cache enabled]	2E-4	---	BNL	No LU>90	Microlatchup @ LET>20, <1E-4 cm2. Moran, LaBel et al, RADECS95 p.263
							See "Table of SEUs-Cache Enabled vs Disabled" in Ref.					Same as above. Proton data exist
3	TAM	80486DX4	MicroP (32-bit)	BiCMOS [3.3V] 0.6 mic.	INT	various	3.5 [cache enabled]	3E-4	---	TAM	LU(th)= ~40.	Eight error modes seen. Kouba & Choi, Test Report Dec. 30, 1996
							6.5 [cache disabled]	3E-5	---			Same as above.
3	CNES	T805	Transputer (32-bit)	CMOS	ISM	Static & dyn.	~2 Worst case: dyn+cache enabled	1000 (reg.); 500 [cache]		IPN	LU(th)=36.	Bezerra, RADECS95 preprint. Dyn=short applications, static=register/RAM
3	IBM	RAD6000 Fixed Pt	MicroP (32-bit)	RHCMOS-E 'CMOS/epi	Loral/FSC	1 of 5 chips	15	---	12	BNL	No LU>120	For worst case >120 deg C. FXPT chip simulates RH RSC6000. Haddad, 1/93
3	A	68HC811	MicroP (32-bit)	CMOS	MOT	—	3	3E-3	—	88-in	LU(th)=8; 8E-3 cm2	Koga ~1995
3	MOT	MPC603 Power PC	MicroP (32-bit)	HCMOS	MOT	reg & cache	2 (reg); 1.5(cache)	----	70(reg); 24 (data cache)	-----		Test ions went up to LET=28. Joe Hockmuth, private com. (cross section vs LET.)
3	A	XC68302	MicroP (32-bit)	CMOS	MOT	—	3	5E-4		88-in	LU(th)=15; 6E-3 cm2	Koga ~1994
3	A	XC68302	MicroP (32-bit)	CMOS	MOT	—	—	—		88-in		Koga. SEU & SEL data exist
Controllers, DSPs, FIFOs & Other Processor-Related Devices												
5	A	SH451	SCSI Controller	CMOS	CIR	—	—	—	—	88-in		Koga. Latchup test only
5	A	68HC811	Microcont. (8-bit)	CMOS	MOT	—	3	3E-3	—	88-in	LU(th)= 8; 8E-3 cm2.	Koga
5	GDD	M82C59A	Priority Interrupt Controller		HAR	interrupt mismatch	11.4	3E-4	—	BNL	No LU>80.	LaBel et al, 96 IEEE Workshop Record.
5	GDD	82380-16 & -20/B	DMA Cont. (32-bit)	CHMOS III 1.5 mic.	INT	900	3.4	>1E-4	Boot talk & normal ops	BNL	LU(th) =~12;~1E-5 cm2.	LaBel, IEEE92 Workshop. Also Moran, RADECS95, p263
5	GDD	82C54	Timer	—	INT	reference mismatch	9	3 E-4		BNL	No LU>80	LaBel et al, 96 IEEE Workshop Record
5	GDD	D8255A-5	Programmable Peripheral	Interface	INT	Output mismatch	<3 6(data);	6 (spikes)		BNL	LU(th)=60	LU may be two current spikes >100 mA. LaBel, 96 IEEE Workshop Record
5	A	AMAS29C1FB	MicroP slice	CMOS	PLS	—	>120	—	—	88-in	No LU >120	Koga
6	A	ADSP2100AGU	DSP (16-bit)	CMOS	ADI	4 tests	7	~2E-4	---	88-in	LU(th)=10 to 18; 3E-4 cm2	DC8950. Koga et al, IEEE TNS, 2982 (Dec., 1996)
6	A	ADSP2181ES & -KS	DSP (16-bit)	CMOS- 0.6 mic. feat.	ADI	4 tests	4	2E-4 (ALU register)	10 (memory)	88-in	LU(th)= 4; ~3E-3 cm2.	DC9513. Koga et al, IEEE TNS, 2982 (Dec., 1996)
6	CNES	ADSP21020	DSP (32-bit Flt. Pt.)	—	ADI	Rgstr. & app.	4	5E-3(static register)	100 (reg)	IPN	LU(th)>13 & <36; 3E-2 cm2	SEU mostly address errors. Bezerra, RADECS95 p.296
6	A	DSP32C	DSP (32-bit)	CMOS	ATT	4 tests	16	~3E-3	---	88-in	LU(th)=40 to 55; 5E-6 cm2	DC9191. Koga et al, IEEE TNS, 2982 (Dec., 1996)
6	CNES	96002	DSP (32-bit Flt. Pt.)	CMOS/bulk,12 & 15 mic epi	MOT	Rgstr. & app.	1.7	SEU masked by latchup.	Data slippages.	IPN	LU(th)=12; 0.1 cm2	The 12-mic version has reduced LU. Bezerra, RADECS95 p.296
6	NRL	320C26	DSP (16-bit)	—	TIX	—	—	—	—	BNL	LU(th) <<29.5,1E-2 cm2	Limited test for LU. Stapor, memo for test of Feb 93
6	A	TMS320C30GB	DSP (32-bit)	CMOS/epi (13 mic.)	TIX	4 tests	3	8E-4 WC registers	—	88-in	LU(th)=10; ~3E-3 cm2	DC: 9050, Koga et al, IEEE TNS, 2982 (Dec., 1996)
6	A	SMX320C30GB	DSP (32-bit)	CMOS/epi (6.5 mic.)	TIX	4 tests	3	8E-4 WC registers	---	88-in	LU(th)=10; ~3E-5 cm2.	DC: 9210, Koga et al, IEEE TNS, 2982 (Dec., 1996)
6	A	SMJ320C30GB	DSP (32-bit)	CMOS/epi (5 mic.); 0.8 feat.	TIX	4 tests	3	8E-4 WC registers	—	88-in	See remarks	Snapback(th)=~5; ~5E-7 cm2. DC: 9543, Koga et al, IEEE TNS, 2982 (Dec., 1996)
6	A	DSP16510A	FFT Proc (16-bit)	CMOS	PLS	OSP only	3	1 E2	—	88-in	LU(th)=3;3E-4cm2	Koga et al, IEEE TNS, 2982 (Dec.,1996)
6	GDD	80387-20/B	Coproc (32-bit)	CHMOS IV 1.0 mic.	INT	—	3.4	1.5E-4	—	BNL	LU(th)=39 to 60;2E-5 cm2	An 80386 peripheral. Moran, RADECS95, p. 2S.2
6	GDD	80387-20/B	Coproc (32-bit)	CHMOS IV	INT	Custom S/W	~10	—	—	BNL	LU(th)=~32	Microlatchup only. LaBel, 96 IEEE Workshop Record
9	—	67201E (Temic)	FIFO (512x9)	CMOS	MTA	—	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9	—	67202E (Temic)	FIFO (1Kx9)	CMOS	MTA	—	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9	—	67203E (Temic)	FIFO (2Kx9)	CMOS	MTA	—	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9	—	67204E (Temic)	FIFO (4Kx9)	CMOS	MTA	—	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9	—	67205E (Temic)	FIFO (8Kx9)	CMOS	MTA	—	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996

Table

Test Org	Device	Function	Technology	Mfr.	Tested Bits	Effective SEU LET Threshold MeV/(mg/cm2)	Device SEU Cross Section (cm2)	Cross Section Per Bit (sq mic)	Facility	Latchup LU) Data--- LET threshold & device cross section. MeV/(mg/cm2) & cm2	Remarks
Logic, Buffers & Phase Lock Loops (See also "Other Linear Devices")											
7 J	74LVQ244	3V Buffer	CMOS/epi	NSC	—	—	—	—	BNL	No LU>120	Test @ 90 deg. C 4/96
7 J	LVC245	3V octal buffer	—	PHL	—	—	—	—	BNL	LU(th)=85	With latchup current >50mA 4/96
7 J	LV244	3V buffer driver	—	PHL	—	—	—	—	BNL	No LU>120	Test @ 90 deg. C 4/96
7 J	F100331	D-FF	Bipolar/ECL(100K)	NSC	Triple	10	1.7E-4	1000	BNL	No LU>85.	Nichols et al June 93
7 A	F100331	D-FF (master/slave)	Bipolar/ECL (1 mic epi)	NSC	Triple	~3	5 E-4	2700	88in	No LU>65.	DC 9220. F100K300 technology family. Koga et al., IEEE95, p1823
7 A	F100341	Shift reg. (8 F/F)	Bipolar/ECL (1 mic epi)	NSC	—	~3	1 E-3	1000	88in	No LU>95	DC 9220. Koga et al., IEEE95, p1823
7 J	CD4014	Shift Register	CMOS	HAR	—	>120	—	—	BNL	No LU>120	Test@ 125deg. C. DC 9403. Test of newer vintage CD4xxx. April 96
7 J	CD54HC4046	Phase Lock Loop	HCMOS/bulk-3.0 mic.	HAR	—	—	—	—	BNL	No LU>120.	Tested 4/95.
7 J	54HC4046	Phase Lock Loop	HCMOS/bulk-3.5 mic.	NSC	—	—	—	—	BNL	No LU>120	Tested 4/96
Static RAMs (SRAMs) sorted by Manufacturer											
9 A	CY100E474	SRAM	Bipolar/ECL	CYP	1Kx4	~3	1 E-2	370	88in	No LU>60.	DC 9010. Koga et al., IEEE95 p1823.
9 A	MBM10474A	SRAM	Bipolar/ECL	FUJ	1Kx4	<<3	3 E-2	730	88in	No LU>40.	DC 8802. Koga et al., IEEE95 p1823
9 Soreq. Isr.	HM65162	SRAM	CMOS/no epi	HAR	2Kx8	3.5 to 4	~5E-2 (1)	—	KOF	LU=4.5-8.5; 2E-2 cm2.	Low energy ions. DC's 85,86,91. Levinson, RADECS95.
9 GDD	HM628128	SRAM	CMOS; NMOS periph.	HTC/Elmo	128Kx8	~1.4	—	—	BNL	No LU>52.5	LaBel et al, 96, IEEE Workshop Record
9 J	L7C199DC-35	SRAM	CMOS	LDI	32Kx8	—	—	—	BNL	LU(th)<<37	LU threshold was not found. 4/96.
9 CERT-CNES	MT5C1008	SRAM	CMOS	MCN	128Kx8	0.6	1 (worst "all 1's")	with multiple errors	IPN & SAT	No LU >36	Duzellier, Ecoffet et al. High vs medium energy study. IEEE95 p. 1797
9 CERT-CNES	MT5C1008	SRAM	CMOS/epi LCRP	MCN	128Kx8	<1.7; <7 (@10% sat)	2E-3	0.29 chess address	IPN & SAT		Duzellier, Ecoffet et al. p 1797, IEEE95. LCRP=low current resistor process
9 J	MT5C2568-35	SRAM	CMOS/epi (suffix=nsec)	MCN	32Kx8	<1.4	0.03 (worst "all 1's")	—	BNL	No LU >72.	DC 9333 is a later S12 process than ~70's. No giant error clusters. 12/93
9 J	MT5C2568-70	SRAM	CMOS/epi (suffix=nsec)	MCN	32Kx8	<1.4	0.03 (worst "all 1's")	—	BNL	No LU >72.	DC 9237 obsolete S06 process. Giant 32K error clusters @LET>26. 12/93
9 J	MT5C2568C-35	SRAM	S12 process (0.65 mic.)	MCN	32Kx8	<1.45	1E-2	—	BNL	No LU >120	Fabbed at Austin Semiconductor. 4/96
9 —	65162E (Temic)	SRAM	CMOS	MTA	2Kx8	3	—	120	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 —	65262E (Temic)	SRAM	CMOS	MTA	16Kx1	3	—	120	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 CERT-CNES	HM65656	SRAM	SCMOS/epi (high-perf)	MTA	32Kx8	5 (High energy)	0.1	300	IPN & SAT		Duzellier, Ecoffet et al, IEEE95 p.1797. High vs medium energy beam study. DC ES
9 MTA	65656E(Temic)	SRAM	CMOS	MTA	32Kx8	4	—	30	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	65664E (Temic)	SRAM	CMOS	MTA	16Kx1	5	—	20	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	65697E (Temic)	SRAM	CMOS	MTA	64Kx1	5	—	20	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	65697S(Temic)	SRAM	CMOS	MTA	256Kx1	4	—	30	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	67130E(Temic)	Dual Port RAM	CMOS	MTA	1Kx8 Master	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	67132E(Temic)	Dual Port RAM	CMOS	MTA	2Kx8 Master	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	67140E(Temic)	Dual Port RAM	CMOS	MTA	1Kx8 Slave	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	67142E(Temic)	Dual Port RAM	CMOS	MTA	2Kx8 Slave	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	67024E(Temic)	Dual Port RAM	CMOS	MTA	4Kx16	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	67005E(Temic)	Dual Port RAM	CMOS	MTA	8Kx8	4	—	100	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 MTA	67025E(Temic)	Dual Port RAM	CMOS	MTA	8Kx16	7	—	150	Unknown	No LU>100.	TEMIC/Matra MHS Radiation Evaluation Results Table July,1996
9 A	UPB10474	SRAM	Bipolar-ECL	NEC	1Kx4	<<3	0.1	2000	88-in	No LU>40.	DC 8721. Koga et al., IEEE95 p1823.
9 J	PDM41256SA250	SRAM	NSC die	PDM	32Kx8	3.4	—	—	BNL	LU(th)=12; 3E-6 cm2	Latchup masks SEU data. 4/96
9 J	KM684002	SRAM	CMOS	SAM	512Kx8				TAM	No LU>87	Beam is 1961 MeV Xe @ 60 deg angle. Nichols 1/97
9 J	CXK58258AP-1020	SRAM	CMOS	SNY	32Kx8	3	1 E-3	—	BNL	LU(th)=40; 2E-6 cm2	Tested 4/96
Dynamic RAMs (DRAMs) sorted by Manufacturer											
10 GDD	MB8116400-60PJ	DRAM	CMOS	FUJ	16Mx1	<1	—	10 to 20	BNL & UCL	No LU>110.	Row errors noted. Harboe-Sorensen IEEE95 Workshop, p 42
10 GDD	LUNA-ES2	DRAM	—	IBM	4Mx4	<3.4	—	—	BNL	No LU>80	Functionality interrupt (SEFI) @ LET=50. DC 9337. Vcc=5V. LaBel, IEEE TNS, 2974 (12/96)
10 GDD	011640OJ1C-70 rev C	DRAM	CMOS	IBM	4Mx4	3 (cell);5 (block)	7E-2 @ LET=50	—	BNL	No LU>11.5.	EEE Links (3/97)
10 CERT-CNES	MT4C4001	DRAM	DC 9248	MCN	1Mx4	<0.4 to <1.7	1	50 to 150	IPN & SAT	No LU>50.	Vcc=5V. Block= rows or columns. LaBel et al, IEEE TNS 2974 (Dec., 1996)
10 ESA	MT4C4M4B1DW	DRAM	CMOS	MCN	4Mx4	<1	—	10	BNL	LU(th)=53. See remarks.	Duzellier, Ecoffet et al, IEEE95 p.1797. High vs medium energy beam study.
10 GDD	MT4C4M4B1DW	DRAM	CMOS	MCN	4Mx4	<1.4	0.2	—	BNL	LU 12 to 26; 2E-4cm2.	Row errors =2E-4 cm2. DC=9406B. Harboe-Sorensen, IEEE95 Workshop, p 42
10 A	M5M44100	DRAM	CMOS	MIT	4Mx1	<3.3	1.0 @ LET=60	—	88-in	No LU>60.	DC 9404. Vcc=5V. LaBel et al, IEEE TNS 2974 (Dec., 1966)
10 J	M5M467800AJ	DRAM	CMOS	MIT	64M	—	—	—	BNL	LU ~60. See remarks.	Compare following. Koga 12/94
10 J	MDM14000GMB-80	DRAM (Mostek package of MIT M5M44100 die.)			4Mx1	—	—	—	TAM	No LU>87	1.2E-6 cm2 [unsat. @ LET=82]. Parts were only partially operational. 3/26/97
10 ESA	KM44C4000J-6	DRAM	CMOS	SAM	4Mx4	<1	—	20	BNL & UCL	No LU>110.	No observable stuck bits. Compare other entry. 11/95
10 GDD	KM44C4000AJ-7	DRAM	CMOS	SAM	4Mx4	<1.4	3 @ LET=110	—	BNL	No LU>110.	Row errors noted. Harboe-Sorensen, IEEE95 Workshop Record, p42
10 ESA	KM41C16000J	DRAM	CMOS	SAM	16Mx1	<1	—	20	BNL & UCL	No LU>110.	SEFI @ LET=60; stuck bits @ LET=60. LaBel, IEEE TNS 2974, (12/95)
10 J	KM48V8004AK-6	DRAM	CMOS (unverified)	SAM	64M	—	—	—	BNL	LU(th)=56 +/- 4 & remarks.	Row errors noted. Harboe-Sorensen, IEEE95 Workshop Record, p42.
											LU cross section is1.3E-6 cm2 [unsat. @ LET=60] 3/26/97

Table

Test Org	Device	Function	Technology	Mfr	Tested Bits	Effective LET MeV/(mg/cm2)	SEU Device (cm2)	SEU Threshold Per Bit	Cross Section (sq mic)	Facility	Latchup LU) Data--- Section device cross section MeV/(mg/cm2) & cm2	Remarks LET threshold &
10 CERT-CNES	SMJ44100	DRAM	Date Code ES	TIX	4Mx1	<0.4	—		>24	IPN vs SAT		Duzellier, Ecoffet et al IEEE95, p 1797 High vs medium beam energy study
10 GDD	TMS416400	"DRAM		TIX	4Mx4	-2	—			BNL?		EEE Links (3/97)
10 ESA	TMS416400A	DRAM	,9.2	TIX	4Mx4	-.1			Preference for 1 to 0	BNL	N o LU>75 See remarks	Row errors =1 E.4 cm2/device Harboe-Sorensen IEEE95 Workshop, p 42
10 GDD	TMS416400DJ-60	DRAM		TIX	4Mx4	"3	—		—	BNL? " - "		Proton upsets also EEE Links (3/97)
10 CNES/ALC	TMS416400- Rev B	DRAM	CMOS/epi(0.5 mic)	TIX	4Mx4	<<17	5		'Row errors .1 E-4 cm2	BNL/IPN	No LU>57	Loss d functionality LET=25 5E-5 cm2 Also half row errors Calvel IEEE94
10 CERT-CNES	SMJ416400-Rev B	DRAM	CMOS/epi(0.5 mic)	TIX	4Mx4	-5 (W C all 1's)	5		—	IPN vs SAT		Duzellier, Ecoffet et al IEEE95 p 1797 High vs medium beam energy study
10 GDD	TC517400J-6	DRAM	CMOS	?0s	4Mx4 <1	4	3 @ LET=100	18		BNL	No LU>100	No stuck bits no multiple errors Vcc=5V La Bel, IEEE TNS, 2974 (12/96)
10 WU	TC51832p	DRAM	planar cell (cap & X1r) T O	S256K	-	2	(ion microprobe)			WAS		Matsukawa preprint Data from He ion microprobe, IEEE, July 1996 —
Flash Memories (Flash EEPROMs)												
12 ESA	28F010-120JC	Flash Memory	CMOS	AMD	128Kx8 7	to 12 (erasures)			—	BNL	No LU>54;<1E-6 cm2	R e a Ecoffet, Only 94 & ESA Rept EWP-1859 (1/96)
12 E s i	CAT28F010P-12	Flash Memory	CMOS	CAT	128Kx8	29 (word errors) Erased @ LET.1			—	BNL	No LU>74	DC1990 1K page errors @ LET= I 1 (read mode) ESA Rept EWP-1859
12 NASA	DPZ1 28x16A3	Flash Memory	CMOS-2 128Kx8 dice	HTC	256Kx8	Only LU observed			—	BNL	LU(th)=20 -1 E-4 cm2	No current 5/93 Pat M O'Neill Part listed as "Dense Pack"
12 ESA	P28F010-120	Flash Memory	CMOS	INT	128Kx8	>74	<1E-6			BNL	LU(th)~23	LU occurs with no loss in stored content (read mode) ESA Rept EWP-1859 (1/96)
12 ESA	28F010	Flash Memory	CMOS	INT	128Kx8	12.7 (transients?)				BNL	LU(th)~.12 7;~1E-4 cm2	Read Only R Ecoffet, June '94
12 NRL	28F010	Flash Memory	CMOS	INT	128Kx8	—	—	—	BNL		LU(th)<<29 5, 2E-3 cm2	Limited LU test Stapor memo for test of Feb 93
12 J	28F016SV	Flash Memory	ETOX, Smart Voltage	INT	2Mx8	For shielded microC, only SV has individual SEUs T A M						Tested @ VDD=3 3V, Vp= 12V 12/96 See H Schwartz IEEE97
12 J	28F016SV	Flash Memory	ETOX,Smart Veil.qe	INT	2Mx8	16 Lockup	2E-6 (control errors); 1 E-5 for 205 mA			BNL/TAM	delayed discharge-- 205 mA	No memory cell errors at BNL-- 3/97 Short current up & down spikes 5/97 See H Schwartz IEEE97
12 J	28F016SA	Flash Memory	ETOX,70 ns access	INT	2Mx8	24 Lockup	5E-6 (control errors); LET=120 for 205 mA			BNL/TAM	delayed discharge-- 205 mA	No individual memory errors Read & write lockup, partial & total byte flips ? & 12 96 H Schwartz IEEE97
12 GDD	28F016SB	Flash Memory	—	INT	16M	9. i1 (incomplete writes, error blocks during writes), sporadic bit flips (read mode)				BNL	LU(th)=26l02'3 <1E-6 cm2	LaBel et al, 96 IEEE Workshop Record
12 ESA	P28F512-120	Flash Memory	CMOS	INT	64Kx8	>74	<1E-6			BNL	LU(th)~23	LU occurs with no loss in stored content (read mode) DC1 990 ESA Rept EWP- 1 859 (1/96)
12 ESA	M5M28F101 P-12	Flash Memory	CMOS	MIT	128Kx8	37 (read mode)	5E-7 (transients)		—	BNL	No LU>74<5E-7 cm2	Read mode Various error types R Harboe-Sorensen, ES A/ESTEC Rept EWP-1 859 (1/96)
12 J	JN16000	Flash Memory	CMOS (unverified)	SAM	16M	26 [read mode]	1 E-6 [read mode]		—	BNL	No LU>60	N o errors ,. memory Current deltas, lockups, page flips, stuck bits & more H Schwartz IEEE97
12 J	KM29N32000	Flash Memory	CMOS (unverified)	s AM	32M	37 [read mode]	2E-6 [read mode]			BNL	No LU>60	No errors in memory Current deltas, lockups, page flips, device flips & more H Schwartz IEEE97
12 ESA	M28F101-150PI	Flash Memory	CMOS	STM	128Kx8	27 (transients)	1 5E -6 (transients)		—	BNL	No LU>74	Transients at LET<37 (read mode) ESA Rept EWP-1 859 11/96)
12 ESA	TMS28F512-120C3NL	Flash Mem	CMOS	TIX	64Kx8	>74	<5E-7			BNL	No LU>74	Transients at LET=3 7 (read mode) DC1992 Esa Rept EWP-1859 (1/96)
Programmable Read Only Memories (PROMs)												
12 BDS	CY7C261	PROM	CMOS	CYP	8Kx8	<15 [latchup]	1 E-3			88-in?	LU<15;~7E-4 cm2	Tested @ LET=37, Normand et al, 95 IEEE Workshop Record p33
12 —	UT28F64	PROM (antifuse-based)	CMOS	UTM	8Kx8				—	Unknown	No LU>1 2R	Anthony Jordan, UTMC News (7/96)
12 ESA	28C1024	EEPROM	—	ATM	64Kx16	<11 (write)	4E-5		Trants, word & block	BNL	No LU>37	D C 1B9131A Harboe-Sorensen, ESA/ESTEC Rept No EWP1859 (1/96)
12 JH	HN58C1001	EEPROM	CMOS/epi	HTC	128Kx8	20(write),>120 (read & static)	2E-5cm2 (write) per device			BNL	N o LU>120	Kinnison, memo 6/95 Compare to GOD data ,. earlier compendium
12 MMS	MEM8129	EEPROM	CMOS with MNOS	HTC(HYB)	328Kx8	4 to 10	1E-3/critical errors for worst case "write")			GANIL	No LU>80	Compare to BNL data below No hard errors DC 9322 Poivey IEEE94
12 ESA	MEM8129W-20	EEPROM	HYB fabbed HTC58C1000 die		128KK8	12 (write)	2E-4 (write)		—	BNL	No LU>53	OC 9318 Harboe-Sorensen, ESA/ESTEC Rept No EWP1859 (1/96)
12 GDD	SA28C256ARP	EEPROM	CMOS	SPE	32Kx8	> 1 5 [LU obscures it]			—	BNL	LU(th) is 15!026	LaBel et al, 96 Workshop Record
12 GDD	SA28C256ERPDB	EEPROM	CMOS/epi	SPE	32Kx8	7(write),11(read);>80(static)			—	BNL	LU>90	LaBel et .1,96 Workshop Record
12 ESA	28C64C-20P1	EEPROM	—	STV	8Kx8	<11(read); >3(write)			—	BNL	LU(th) >11 & <37, 5E-6 cm2	DC9248 Harboe-Sorensen, ESA Rept EWP-1859
12 ESA	28C010D-20	EEPROM	—	XIC	128Kx8	<1 5	>>5E-5 @ LET=3		—	BNL		Only low LET ions DC 9236 Harboe-Sorensen, ESA/ESTEC Rept EWP 1859 (1/96)
12 ESA	28C512D-15	EEPROM	—	XIC	64Kx16	<~1 5 (write)	>>3E-5 @ LET=3		—	BNL		Only low LET ions DC 9144 Harboe-Sorensen, ESA/ESTEC Rept EWP-1859 (1/96)
12 ESA	CY7C263-25PC	UVEPROM	—	CYP	8Kx8	<<26 (Address errors)			—	BNL	LU(th) <<26;>2E-5 cm2.	DC9224. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	HN27C256HG-70	UVEPROM	—	HTC	32Kx8	<<26 (transients)			—	BNL	LU(th)= 60 to 82, 6E-7 cm2	DC9212. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	M5M27C256K-12	UVEPROM	—	MIT	32Kx8	<<26 (transients)			—	BNL	No LU>82.	Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	M27C256B-15XFI	UVEPROM	—	SGS	32Kx8	masked by latchup			—	BNL	LU(th) <<26, ~1E-5cm2	DC9222. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	TC57256AD-12	UVEPROM	—	TOS	32Kx8	<<26 (transients)			—	BNL	No LU>82.	DC9202EBI. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	M27C512-15I	UVEPROM	—	SGS	64Kx8	masked by latchup			—	BNL	LU(th) <<26;1E-5 cm2	DC9214. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	SMJ27C512-20JM	UVEPROM	—	TIX	64Kx8	<<26 (transients)			—	BNL	No LU>82.	DC9224A. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	HN27C101AG-15	UVEPROM	—	HTC	128Kx8	26 to 60 (transients)			—	BNL	No LU>82.	DC9202. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	M5M27C101K-15	UVEPROM	—	MIT	128Kx8	<<26 (transients)			—	BNL	No LU>82.	Reno Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	TMS27C010A-15	UVEPROM	—	TIX	128Kx8	masked by latchup			—	BNL	LU(th) <<26, 4E-6 cm2	DC9222. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	D27C010-150V10	UVEPROM	—	INT	128Kx8	masked by latchup			—	BNL	LU(th) <<26;1E-6 cm2	Die mark=1988. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	M27C1001-15FI	UVEPROM	—	SGS	128Kx8	<<26 (transients)			—	BNL	No LU>82.	DC9227E5S. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	D27C2001D-15	UVEPROM	—	NEC	256Kx8	masked by latchup			—	BNL	LU(th) <<26, 2E-5 cm2	DC9150. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	M27C4001-12FI	UVEPROM	—	SGS	512Kx8	<<26 (transients)			—	BNL	No LU>82.	DC9240B. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	TC574000D-150	UVEPROM	—	TOS	512Kx8	60 to 82 (transients)			—	BNL	No LU>82.	DC9042EAK Harboe-Sorensen, ESA Rept EWP-1859 (1/96)
12 ESA	SMJ27C040-12JM	UVEPROM	—	TIX	512Kx8	26 to 60 (transients)			—	BNL	No LU>82.	DC IDL9226AI. Harboe-Sorensen, ESA Rept EWP-1859 (1/96)

Table

Test	Org	Device	Function	Technology	Mfr	Tested Bits	Effective SEU LET Threshold MeV/(mg/cm2)	Device SEU Cross Section (cm2)	Cross Section Per Bit [sq mic]	Facility	Latchup (LU) LET threshold & device cross section MeV/(mg/cm2) & cm2	Data--- Remarks
Application Specific ICs (ASICs), Programmable Array Logic (PAL) & Field Programmable Gate Arrays (FPGAs)												
13	NRL	388052	ASIC		LIT	---	—	—		BNL	LU(th)<<29 5, 1 E-3 cm2	Limited LU test Stapor memo for test of Feb 93
13	A	"03215 &Q3236	ASIC (PLL)	BiCMOS	QLC	—	1	1 E.3 (phase upset); 3E-4 (freq upsets)		88-in	No LU>65	Both devices have same response Jobe et al, IEEE- NS, 28S8 (12/96)
14	GDD	A1020B	FPGA	CMOS/epi (0.9 mic.)	ACT	—	28	—	200	BNL	LU(th)=55.	R. Katz, EEE Links, Nov., 96. "The only Actel device known to latchup."
14	J	1020B	FPGA	CMOS/epi (TIX chip)	ACT	—	—	—	—	TAM/BNL	LU(th)<<25;2.3E-5cm2.	Swift: "TIX is very latchable." TAM=12/96 & BNL=11/96.
14	GDD	RH1020	FPGA	CMOS/epi (1.0 mic.)	ACT	—	—	—	—	BNL	No LU.	SEDR. R. Katz, EEE Links, Nov 96.
14	A/GDD	A1280A	FPGA	CMOS/epi (1.0 mic.)	ACT	1232 mods.	28(C), 5(S)	—	800(S) & 200(C)	88-in.	No LU>100.	A: SEDR. C=combinatorial, S=sequential logic. R. Koga 93. GDD 11/96
14	GDD	A1280A 3.6V	FPGA	CMOS/epi (1.0 mic.)	ACT	—	—	—	—	BNL	No LU.	No SEDR. R. Katz, EEE Links, Nov 96.
14	ESA	A1280A	FPGA	CMOS ACT2 (MAT chip)	ACT	1232 F/F's	27(C 0's), 10(S 1's & I/O 1's) @ 1%		1500(S) & 300(C & I/O)	BNL	No LU >120.	C=combinatorial, S=sequential logic. S. Mattsson, ESA Report SE/REP/0047/K, 9/96
14	GDD	A1280XL	FPGA	CMOS/epi (0.6 & 0.8 mic.)	ACT	—	—	—	—	BNL	No LU.	SEDR. R. Katz, EEE Links, Nov 96.
14	GDD	RH1280	FPGA	CMOS/epi (Rad Hard)	ACT	—	22(C), 3(S)	—	800(C) & 900(S)	BNL	No LU.	SEDR. Proton upsets for S-module. R. Katz, EEE Links, Nov 96.
14	ESA	RH1280	FPGA	CMOS/epi (Rad Hard Loral)	ACT	1232 F/F's	27(C 0's),10(S 1's), 15(I/O 1's) ---		170(C) & 600(S) & 100	BNL	No LU >120.	C=combinatorial, S=sequential logic. Protons. Mattsson, ESA Rept SE/REP/0047/K, 9/96
14	ESA	RH1280 3.3V	FPGA	CMOS/epi (Rad Hard Loral)	ACT	1232 F/F's	15(C 0's), 6 (S 1's), 10(I/O both) ---		400(C) & 1000(S) & 20	BNL	No LU >120.	C=combinatorial, S=sequential logic. Protons. Mattsson, ESA Rept SE/REP/0047/K, 9/96
14	GDD	A1460A	FPGA	CMOS/epi (1.0 mic.)	ACT	—	21(C),8(S & I/O) —		~20(C) & 100(S)	BNL	No LU.	SEDR. Proton upsets for S-module. R. Katz, EEE Links, p17, July 96.
14	GDD	A1460A 3.3V	FPGA	CMOS/epi (1.0 mic.)	ACT	—	25(C), 6(S)	—	80(C) & 200(S)	BNL		R. Katz, EEE Links, p17, July 96.
14	ESA	A1460A	FPGA	CMOS ACT3 (MAT chip)	ACT	—	32(C 0's), 8(S 1's, 10 (I/O) ---		150(C) & 1000(S) & 2(	BNL	No LU >120.	C=combinatorial, S=sequential logic. Protons. Mattsson, ESA Rept SE/REP/0047/K, 9/96
14	ESA	A1460A 3.3V	FPGA	CMOS ACT3 (MAT chip)	ACT	—	20(C 0's), 6(S 1's), 8(I/O) ---		300(C) & 2000(S) & 7(	BNL	No LU >120.	C=combinatorial, S=sequential logic. Protons. Mattsson, ESA Rept SE/REP/0047/K, 9/96
14	GDD	A14100A	FPGA	CMOS/epi?	ACT	—	21(C),8(S & I/O) —		100(C)	BNL	No LU.	No LU. SEDR. R. Katz, EEE Links, Nov 96.
14	GDD	AT6002-JC	FPGA	CMOS/epi 0.8 mic	ATM		7 to 8(data & reconfig.)		—	BNL	LU(th)= ~11	R. Katz, EEE Links, LaBel 96 IEEE Workshop Record Proton upsets also
14	GDD	ATT2C04-2 ORCA	FPGA	CMOS 0.5 mic feature	ATT	—	<7 9(config),>10(data) ---		—	BNL	LU(th)< 7.9	R. Katz, EEE Links, p17, July 95, LaBel, 96 IEEE Workshop Record
14	GDD	RH1280	FPGA	CMOS 0.8 mic feature	LFS		22(C), 3(S)	—	800(C), 900(S)	BNL		R.Katz, EEE Links, p17, July, 1996.
14	GDD	CLAY-31	FPGA	SRAM-based	NSC	—	5		7(SER), 80 (Data)	BNL	No LU>60	SER = SEU in the configuration cell R.Katz, EEE Links (11/96)
14	GDD	XC3090A	FPGA	CMOS/bulk	XIL	—	4 to 7 (SEU & latchup)		—	BNL	LU(th)= 4 to 7	R. Katz, EEE Links, p17, July, 1996, LaBel, 96 IEEE Workshop Record
15	GDD/PREL	UT22VP10	PAL	RADPAL CMOS 1.2 mic	UTM	—	~60	—	—	88-in	No LU>109	Amorphous S, based R.Katz, EEE Links, summarizes Boeing data 11/96
15	GDD	UT22VP10	PAL	RADPAL	UTM	—	37	—	—	BNL	No LU>90	LaBel et al, 96 IEEE Workshop Record
Other Linear Devices												
18	GDD	AM7968 & AM7969	TAXI Transmitter & Receiver	Bipolar	AMD	—	<3.4	—		BNL	No LU >53	LaBel, IEEE93 Workshop Record & EEE Links (3/97)
18	J	AD485AQ	Transceiver	CMOS	ADI	—	—	—		TAM	No LU>152	Test @ 90 deg C 12/96
18	J	AD1485	Transceiver	CMOS	ADI		—	—		TAM	No LU>90	Test @ 88 deg C 12/96
18	J	LTC1480	3.3V Transceiver	CMOS	LTN			—		TAM	No LU>152	Test @ 25 deg C 12/96
18	J	LTC1487	Transceiver	CMOS	LTN		—	—		TAM	LU(th)<45,2 E-7 cm2	Tested 12/96
18	J	MAX485E	Transceiver	CMOS	MAX	—		—		TAM	No LU>152	Test @ 25 deg C 12/96
18	J	MAX3485	3.3V Transceiver	CMOS	MAX	—	—	—		TAM		No LU>152 @ 25 deg C SEL at LET=152 @ 90 deg. c 12/96
18	J	32C278TM	Transceiver	CMOS	NSC	—	—	—		TAM	No LU>152	Test 0 25 deg c 12/96
18	J	SP485ES	Transceiver	CMOS	SIP	—	—	—	—	TAM	See remarks	No LU>152 @ 25 deg C LU(th) =152 0 90 deg. C 12/96
18	J	SN75LBC176	Transceiver	CMOS	TIX		—		—	TAM	See remarks	No LU >45088 deg C. LU(th) =90 @ 67 deg. C. 12/96
18	GDD	UT63M147-BPC	1553 transceiver	Bipolar?	UTM	—	11		—		No LU>35	LaBel, EEE Links (March,1997)
18	GDD	QS3384DM	Bus quickswitch Unk		Qs1	—	—	—	—	BNL	LU(th) =15 to 18	LaBel et al, 96 IEEE Workshop Record
18	J	RH1056	Op Amp	RH bipolar & JFET input	LTN	0.5V & other inputs. A reverse input polarity reverses output transients.				TAM		Transients for LET(th)=2, 4 1. 8V for - 1 5 microsec; 1E-3 cm2 @ LET=44 8/95 & 1 1/95
18	Op Amp	RH1056	Op amp	RH bipolar & JFET input	LTN	—	45 (transients)	1 E-3	—	BNL	No LU >60	Transients for LET(th)=3, amplitudes of 1 5V to 2 5V for 51. 10 microsec
18	Op Amp	LM108A		Bipolar	LTN	Neg 0.5V in gives	13	V transient for 14	microsec	TAM	+ 0.5V in 5V for 10	Transients for L E) T th <<7 W d e amplitude variability at LET=44; 6E-4 cm2 1 1/95
18	J	RH108A	Op Amp	rad hard bipolar	LTN	Very similar to non rad hard tests of same given above				TAM		Transients for LET(th) <<7, 6E-4 cm2 at LET=44 11/95
18	A	UC1R02	PWM (low P current)	BiCMOS	UTR	—	1 several SEU modes	5 E-4	—	88in	No LU>63	Penzin et al, IEEE-TNS 2968 (Dec 1996)
18	ALC	UC1806	PWM [1 846 equiv.]	BiCMOS	UTR	—	—	—	—	BNL	No LU >119	NoSEB>11 9 DC/DC reset errors are "not acceptable for any space application."
18	A	UC1825A	PWM (high freq.)	Bipolar	UTR	—	1 several	SEU modes 1 E-2	—	88,"	No LU>63	Penzin et al, IEEE-TNS 2968 (Dec.,1996)
18	A	UC1845A	PWM (current mode)	Bipolar	UTR		1 several SEU modes	2 E-4		88in	No LU>63	Penzin et al, IEEE-TNS 2968 (D.cc,,-99-)
18	HAC	BiCMOS 03216	PWM (no	CMOS)	OAL		1	2 E-3	—	88in	No LU Serial &	Parallel modes rox same Jobe, IEEE96 preprint
18	HAC	Q3236	PWM	BiCMOS (with CMOS)	OAL	—	1	2 E-3	—	88,.	No LU>62	Serial & Parallel modes approx same Jobe, IEEE96 preprint
18	J	LM111	Comparator	Bipolar	NSC	Test + or - inputs. A transistor output goes from "off" to "on" or vice versa.				TAM		Transients @ LET<<7 swing rail-to-rail, 3E-4 cm2 for 04 microsec Nichols, IEEE TNS (12/96)
18	J	LM139	Comparator	Bipolar	N S C	—	—	—	—	TAM/BNL		Transients @ LET=2, swing rail-to-rail, 6E4 cm2 for 2103 microsec Nichols, IEEE TNS (12/96)
18	J	LM139	Comparator	Bipolar	PMI		—	—	—	TAM		Transients @ LET=1 4, swing rail-to-rail, 7E-4 cm2 for <4 microsec. Nichols, IEEE TNS (12J%)
18	J	TC4428	MOSFET driver	—	TCS	—		—	—	TAM	LU(th)= -24,1	E-6 Latch2 hueasily cause burnout 12/96
18	GDD	MIC4427	MOSFET driver	4426'442714428	family Micrel	—	LU test only (Lat	—	—	BNL	No LU >90	P+ isolations prevent LU Skipper, IEEE95 Workshop Record, p 50
18	BPSRC	DS26C32AMJ	Diff Line receiver	CMOS/thick epi	< 7/92	NSC	—	—	—	88-in	LU(th)=14,1 6E-4 cm2	Tested 0 525~,~d~ C Majewski, Boeing REL Rept RTR-SLH-V1-A
18	BPSRC	DS26C32AMJ	Diff Line receiver	CMOS/thin epi	> 7/92	N S C	—	—	—	88-in	No LU >77	Tested @ 525v, 100 deg. C. Majewski, Boeing REL Rept 0020-RTR-SLH-V2-A (3/94)

Table

Test Org	Device	Function	Technology	Mfr	Tested Bits	Effective SEU "LET Threshold MeV/(mg/cm2)	Device SEU Cross Section (cm2)	Cross Section Per Bit [sq mic]	Facility	Latchup LU) Data--- L E T threshold & device cross section MeV/(mg/cm2) & cm2	Remarks
Analog to Digital Converters (ADCs) & Digital to Analog conveners (DACs)											
19 J	AD7225TO	DAC (8-bit)	LCCMOS	ADI	—	—	—	—	TAM	No LU>62	1 % 1 MeV Xe at 45 deg Runs with PIC16674A microC Nichols, 1/97
19 GDD	DAC8800	DAC (8-bit)	—	ADI	—	" "	">80		—	No LU>80	LaBel, EEE Links(March, 1 ?97)
19 J	MX7545TO	DAC (1 2-bit)	CMOS	MAX	"-	>120	'all' 1's!		BNL	No LU>120	Nichols, 4/95
19 GDD	SP9380	DAC (18-bit)	—	SIP	Ref mismatch	1.45 to 3 4	—		BNL	LU(th)= 371060	Catastrophic LU La Bel, 96 IEEE Workshop Record
19 J	HI1276	A/D (8-bit Flash)	Bipolar- ECL	HAR					BNL	No LU>70	With self heating up to T=69 deg C 3/26/97
19 J	SPT7725	A/D (8-bit Flash)	—	SPT	—				BNL	No LU>120	Used thermo-electric cooler to maintain temp <34 deg C 3/26/97
19 NRL	TMC1	A/D (8-bit Flash)	—	TRW	—				BNL	LU(th)<<29 5, 2E-4 cm2	Limited LU test Stapor memo for test of Feb 93
19 J	AD573	A/D (10-bit)	Bipolar-IIL	ADI	13	—	—	—	88in		Nov 1989
19 J	AD773A	A/D (10-bit)	BiCMOS	ADI		—	—	—	BNL	No LU >120	Test up to 70 deg C, 525V 9/96
19 J	AD12062	A/D (1 2 -	CMOS/epi	ADI					BNL	LU(th)=12;3E-4cm2	Cross section plot shows no saturation at LET=60 3/26/97
19 J	AD574A	A/D (12-bit)	BiMOS	ADI	8 MSB's	<3	1 5E.4 [8 MSB's]	—	88in	No LU >110	Tested Sept 91
19 NWSC/A	AD42961	A/D (12-bit Flash)	RH BiCMOS	ADI		10 offset errors	1 E-5 cm2 per MS (offset);5E-5 cm2 (noise)		88-in	No LU>126	Hard AD87 1 Divide by samples per irradiation Turflinger, IEEE TNS- 4/96
19 NWSC/A	RBC-12 (hard AD8	A/D (12-bit Flash)	RH BiCMOS	ADI		10 offset errors	1 E-5 cm2 per MS (offset),5 E-5 cm2 (noise)		88-in	No LU>126	Need to divide by samples per irradiation, says Turflinger in IEEE TNS- 4/96
19 GDD	CS5012A	A/D (12-bit)	—	CRY	—	3.5 to 4.8	—		—	LU(th)=11	LaBel, EEE Links (March, 1997)
19 J	LTC1419	A/D [14-bit]		LTN	—			—	BNL	No LU>120	Used 1 KHZ sine wave input 3/26/97
19 SPE	ADS7809	A/D(16-bit)	CMOS	BUB	—	18	sE-5		BNL	LU(th)=23; 3E.5 cm2	Layton, P. J. Space Electronics Test Rept (3/27-/97)
19 J (CIT)	DDC101	A/D(20-bit)	CMOS/epi(9 to 11 mic.	Burr Brown	Special Evaluation Fixture for latchup test only				TAM	LU(th)=9 See remarks	1E-5 cm2 0 LET=15 LU currents = 500 mA 11/95 Cal Tech special test
20 GDD	ICL7662MTV-4	Voltage Converter	—	MAX	various Vcc <<60 ,10,Vm.15V]	—	—		BNL	No LU>80	Higher Vcc strew no errors. LaBel et al, 96 IEEE Workshop Record
DC/DC Power Converters											
20 J	ATR2815D	DC/DC Power Converter rad hard IC's etc	LAM(ADA)	—	~24 [~13 ms dropout]	1 E-5 [LET=44]			TAM	No LU>44	Permanent drop out at LET=44;1E-5 cm2. 12/96
20 J	ATW2805S	DC/DC Power Converter CMOS (one IC)	LAM(ADA)	—	~24 [~8 ms. drop out]	1 E-5 [LET=44]			TAM	No LU>44	No permanent dropout at LET=44. 12/96
20 J	MHF2815D	DC/DC Power Converter ---	ITP	—	No errors	—	—		TAM		No errors @ LET>94 [1961 MeV XE @ 60 deg angle]. Input=28V "on" Nichols, 1/97
20 J	MHF2805D	DC/DC Power Converter ---	ITP	—	No errors	—	—		TAM		No errors @ LET>94 [1961 MeV XE @ 60 deg angle]. Input=28V "on" Nichols, 1/97
20 GDD	MCH2805S	DC/DC Power Converter ---	ITP	—	No errors>82	—	—		BNL	See remarks.	No SEEs of any kind LET>82. LaBel et al, 96 IEEE Workshop Record
20 J	2680M-S05F	DC/DC Power Converter hybrid	MDI	---	6 (reset errors)	2E-4 (reset errors)	—		BNL	See remarks.	No destructive cond. @ LET>60. 8/95 Localized component error identified
20 GDD	MDI2680	DC/DC Power Converter hybrid	MDI	---	30 (dropout, needing power cycling)				BNL		LaBel et al, 96 IEEE Workshop Record
20 GDD	MDI2690R-D15F	DC/DC Power Converter hybrid	MDI	---	4 to 8 (reset errors)	5E-4 (reset errors)			BNL	See remarks.	No destructive cond. @ LET>72. IEEE95 p 1957
20 GDD	5690R-D15	DC/DC Converter ---	MDI	---	>83	—	—		—		LaBel, EEE Links (March, 1997)
Network Interface Controllers & Miscellaneous Devices											
21 MMS	DP83932CVF	Network Interface Cont M2CMOS	1 m.	NSC	—	—	—		GANIL/GSI	LU(th)<15;3E-3cm2	DC9442 Poivey et al, IEEE96 Workshop Proton data also
21 MMS	DP83956AVUJ	Network Interface Cont M2CMOS	1 5 . .	N S C	—	—	—		GANIL/GSI	LU(th)=20;2E-4cm2	DC9452 Poivey et al, IEEE96 Workshop Proton data also
21 MMS	DP83950BVQB	Network Interface Cont M2CMOS 1.5 mic	NSC				—		GANIL/GSI	LU(th)=20;2E-4cm2	DC9506 Poivey et al, IEEE96 Workshop
21 MMs	DP8392CV	Transc'vr Interface Lo P Schottky- J Isol	N S C	—	Data errors at LET.!, normalized per transmitted bit ----				GANIL/GSI	No LU	DC9452 Poivey et al, IEEE96 WProtondata also
21 MMS	AM79C98	Twisted Pair Transceiver CMOS	AMD		>42	—	—		GANIL/GSI	LU(th)=50;5E-5cm2	LU cross section O LET=82 DC9545 Poivey et al. IEEE96 Workshop
22 eq Converter ---		AD! Converter ---		—	~7.4	—		—		—No LU >15	LaBet, EEE Links (March, 1997)
22 GDD	AD630	Balanced Modulator	ADI	—	<7.4	—					LaBel, EEE Links (March, 1997)
22 J	AD783	s & H amplifier	ABCMOS=bip & CMOS	ADI	—	—	—		BNL	No LU>120	LU tested up to 125 deg C 8/95 "ABCMOS technology"
22 CNES	IMSCO11	Data link- MicroP peripheral ---	ISM	—	-2	2E-4			IPN	No LU>72.	Bezerra et al, RADECS95 preprint on SEWS in Transpufers
22 J	N/A	Autocorrelator	—	SBI/HPA	—	—			BNL	No LU >120.	Tested Mar 26, 1997
22 J	IMP 50E10	EPAC [Elec Prog Analog Circuit]--	CMOS IMP	daisy chain	11	>>5E-5 (obscured by	latchup at LET=1 5]		BNL	U(thl.15 .1 E-4cm2	Aug 95 EPAC is a configurable group of analog elements
22 GDD	IMP 50E10	EPAC [Elec Prog Analog Circuit]--	CMOS IMP	summing op amps	<1 5	—	—		BNL	LU(th)=15to27	LaBel, 96 IEEE Workshop Record See preceding entry
22 GDD	HSSR-7110	Optocoupler- AlGaAs LED & n-ch MOSFET	HPA	solid st relay	>100	—	-		BNL	No LU>100	LaBel et al, 96 IEEE Workshop Record
22 GDD	HX2300	Soi Test Metal	RICMOS SOI 4	HON	config JK O, RSF/Fs	>120	—		BNL	No LU>120	"A true Rad Hard process" LaBel et al, 96 IEEE Workshop Record

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Appendix /-- Manufacturer Abbreviations

The following is a list of manufacturers who have appeared in all of the compendia of data. Not all of those listed here appear in this year's data set.

ACT Actel Corp.
ADA Advanced Analog
ADI Analog Devices Inc.
AFX Aeroflex Labs
ALS Allied Signal
ALT Altera Corp.
AMD Advanced Microdevices Corp.
APX Apex
ATM Atmel Corp.
ATT American Tel & Tel
BAL Bal Efatrom
BUB Burr-Brown Research
CAT Catalyst
CIR Cirrus Logic Inc.
CPT Crosspoint
CRY Crystal Semiconductor Inc.
CYP Cypress Corp.
DAT Datel
DDC DDC ILC Data Device Corp.
DEC Digital Equipment Corp.
EDI EDI Corp.
ELN Elantec
FAS Fairchild Semiconductor Div.
FER Ferranti
FUJ Fujitsu Ltd.
GAZ Gazelle
GEC General Electric
GEC-PLS Plessey Semiconductors

HAR	Harris Corp., Semiconductor Div.
HTC	Hitachi Ltd.
HON	Honeywell Inc.
HPA	Hewlett-Packard Co.
HYB	Hybrid Systems
IBM	IBM
IDT	Integrated Device Technologies, Inc.
IMP	IMP, Inc.
INM	INMOS Corporation
INT	Intel Corp.
ISM	INMOS Corp.
ITP	Interpoint
LAM	Lamda (from ADA)
LDI	Logic Devices Inc.
LIT	Litton
LTN	Linear Technology
LSI	LSI Logic Corp.
MCC	Microchip
MCN	Micron Technologies
MDI	Modular Devices, Inc.
MED	Marconi Electronic Devices
MIC	Micrel Semiconductors
MIR	Micro-Rel Corp.
MIT	Mitsubishi
MMI	Monolithic Memories Inc.
MOC	Mosaic Semiconductor
MOS	Mostek
MOT	Motorola Semiconductor Products Inc.
MPS	Micro Power System
MTA	Matra Harris Semiconductor
MXM	Maxim Integrated Products
NCR	National Cash Register
NEC	Nippon Electric Corp.
NSC	National Semiconductor Corp.
NTL	Natel Engineering
OKI	Oki Semiconductor, Inc
owl	Omni-Wave, Inc.
PDM	Paradigm Technology Inc .
PFS	Performance Semiconductor Inc.
PHL	Phillips
PLS	Plessey Semiconductors
PMI	Precision Monolithic, Inc.
QLC	Qualcomm Inc.
QSI	Quality Semiconductor Inc.
RAY	Raytheon Co., Semiconductor Division
RCA	Radio Corporation of America
RMT	Ramtron
SAM	Samsung
SBI	Space Borne, Inc.

SEI Seiko
SEQ SEEQ Technology Inc.
SGN Signetics Corp.
SGP Signal Processing
SIE Siemens Components, Inc.
SIL Siliconix
SIP Sipex
SLG Silicon General
SNL Sandia National Laboratories
SNY Sony Corp.
SOR SOREP
SPE Space Electronics Incorporated
SPT Signal Processing Technology
SSD Solid State Devices
STC Silicon Transistor Corp.
STM SGS-Thomson (STM), France
TCS Telcom Semiconductor
TEL Teledyne Crystalonics
TIX Texas Instruments Inc.
TMS SGS-Thomson , France
TOS Toshiba
TRW TRW Inc.
UTM United Technologies Microelectronics Center
UTR Unitrode
WAF Waferscale
WDC Western Digital Corp.
WEC Westinghouse Electric Corp.
XIC Xicor Inc.
XIL Xilinx Inc.
ZOR Zoran
ZYR Zyrel

Appendix II-- Test Organizations

A The Aerospace Corporation; El Segundo, CA
ADI Analog Devices Semiconductor, Wilmington, MA
ALC Alcatel Espace, Toulouse, France
Ball Ball Aerospace Systems Division, Boulder, CO
BDS Boeing Defense & Space Group, Seattle
BPS Boeing Physical Sciences Research Center, Seattle
CERT 2, Avenue Edouard Belin, Toulouse, France
CLM Clemson University; Clemson, SC
CNES Centre National d'Etudes Spatiales; Toulouse, France
DASA Deutsche Aerospace AG, Munich
ESA European Space Agency-- several facilities
GD General Dynamics
GDD NASA Goddard Space Flight Center; Greenbelt, MD
GE GETSCO, Philadelphia
HAR Harris Semiconductor

HAC Hughes Aircraft
HON Honeywell
IBM IBM (now Lockheed Martin Federal Systems)
J Jet Propulsion Laboratory (JPL); Pasadena, CA
JH John Hopkins Applied Physics Laboratory; Laurel, MD
LIN Lincoln Laboratories, M. 1. T.; Cambridge, MA
Loral Loral, Manassas, VA
LLNL Lawrence Livermore National Laboratory; Livermore, CA
MM Martin Marietta Astrospace, Valley Forge, PA
MMS Matra Marconi Space; Vélizy, France
MOT Motorola GSIG, Scottsdale, AZ
NASA National Aeronautics & Space Administration
NRL Naval Research Laboratories, Washington D. C.
NWSC Naval Weapon Support Center, Crane, IN
PHY Physitron , Inc., San Diego
R Rockwell International, Anaheim, CA
SNL Sandia National Laboratory, Albuquerque
Soreq, Isr. See Remarks Column.
SSS S-Cubed, San Diego
TAM Texas A & M University, College Station, Texas
TRW TRW Space and Defense Sector; Los Angeles
UTM United Technologies Microelectronics Center, Colorado Springs
WU Waseda University, Tokyo, Japan

Appendix Ill-- Test Facilities

88-in. = 88-inch cyclotron, Lawrence Berkeley Laboratory, Berkeley, California
BNL= Tandem Van de Graaff, Brookhaven National Laboratory, Long Island, NY
Cf-252 = A Cf-252 fission source. The data from this source is rarely given because of inaccuracies of cross section and threshold inherent to the low energy fission ions.
ESA= European Space Agency -- several sites
GANIL= Cyclotron for High Energy Heavy Ions; Caen, France
GSI= Cyclotron for High Energy Heavy Ions; Darmstadt, Germany
HAR= Van de Graaff at Harwell, England
IPN= Tandem Van de Graaff, Institut de Physique Nucleaire; Orsay, France
KOF= Koffler. Low energy ions.
SAT= Saturne synchrotrons, LNS, Saclay, France
TAM= Texas A & M University- Cyclotron Institute, College Station, Texas
UCL= Cyclone cyclotron, Louvain-la-Neuve, Belgium
UW= Tandem Van de Graaff, University of Washington , Seattle
WU= Waseda University, Japan

Appendix IV-- Update for Reference 6

A data page; inadvertently omitted from Ref. 6, Table 1; is included here, in a format that fits exactly between pages 12 and 13 of Reference 6.

References

[1] D. K. Nichols, W. E. Price, W. A. Kolasinski, R. Koga, J. C. Pickel, J. T. Blandford, A, E. Waskiewicz, " Trends in Pads Susceptibility to Single Event Upset from Heavy Ions," IEEE Trans. on Nut. Sci., NS-32, No. 6, 4189 (Dec. 1985)

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Voice: (81 8)354-1 968
FAX: (81 8)393-4559
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Appendix IV

Table 1 SEU Data

	Test Org.	Device	Function	Technology	Mfr	Bits	Effective LET.. Threshold	Device Cross Section (cm2)...	Cross Section P*, Bit [sq mic]	Facility	Remarks
9	ESA	HM62256	97AM	CMOS	HTC	32Kx8	3	—	200	IPN & BNL	No LU IEEE93 p 1498 CC8641 & 8645 SEU IPN<BNL Proton data exists
9	CNES	HM62256R	SRAM	CMOS	HTC	32Kx8	<1 7	—	300	IPN	No LU IEEE93 preprint DC9303 Proton data exists
9	CNES	HM62382H	SRAM	DC 9249	HTC	32Kx8	1 7	—	40	IPN	No L U IEEE93 preprint DC9249 Proton data exists
9	ESA	HM6264	SRAM	CMOS	HTC	8Kx8	-5	—	1509 LET=13, then LU	BNL	LU(th) <13, 1E-3 cm2 IEEE, p 1498 (Dec 93) DC8431 Proton data exists
9	E SA	HM6264A	SRAM	CMOS	HTC	8Kx8	-5	—	150	IPN	LU(th) <13; 1E-3 cm2 IEEE, p 1496 (Dec 93) DC8901 Proton data exists
9	MMS	MSM8128	SRAM		HTC	128Kx8	—	—	—	GANIL	SHE (Single Hard Error) LET(th)=-50; 1E-3cm2 Poivey, IEEE-NS, 2235 (1994)
9	MMS	HM628128	SRAM	CMOS/epi	HTC	128Kx8	—	—	—	GANIL	No LU> 110 Hard Errors Beaucour, 93 IEEE Workshop
9	GOD	HM628 126	SRAM	CMOS/epi	HTC	128Kx8	<1 4	33 dyn, O 2 static	Multiple bits per strike	BNL	No LU> 110 LaBel 94 IEEE Workshop Record Tested 5/93
9	ESA	HM628 128	SRAM	CMOS	HTC	128Kx8	-3	—	40	IPN	No L U IEEE93 p 1498 DC9009 Proton data exists
9	MMS	HM628128	SRAM	CMOS/epi	HTC	128Kx8	—	—	—	GANIL	No LU>1 10 Hard errors Beaucour, 93 IEEE Workshop
9	J/A	HM628 126	SRAM	NMOS/CMOS	HTC	128Kx8	4	0 6	60	88-in	J LU(th)=80 March 199D A No LU>127 IEEE93 preprint
9	EsA	HM628512	SRAM	CMOS	HTC	512Kx8	-2	—	60	BNL	No LU IEEE93 p 1498 DC9235 A few stuck bits that anneal Proton data exists
9	IBM	2568CRH	SRAM	RHCMOS(Manassas)	IBM	32Kx8	>100	No upset	No upset	BNL	No LU>100 From IBM Rept on Space Station (DMS) 3/93
9	GDD	70V25	SRAM	CMOS	IDT	16 bit wide, dual	<346	—	50.	BNL	No LU>80 Static & dynamic tests Multiple upsets LaBel test of 7,94
9	A,JH	10T71256	SRAM	NMOS/CMOS	IDT	32Kx8	25	0 2	—	88 In & Bevalac	LU=15; 7E-5 cm2 SMU's A Dec 1967 & RADECS93 JH tested Aug 90
9	CNES	IDT7134	SRAM	CMOS	IDT	4Kx8	<1 7	—	300	IPN	LU=12 7; 7E-4cm2 Ecoffet et al, IEEE93 Proton dam exists Date Cods ES
9	IBM	IMS1601EPI	SRAM	CMOS non radhard	ISM	64Kx1	-2	0 4	includes multiple errors	88-in	No LU>60 O'Neill, IEEE, p 1755 (10/94) using data of T Scott (IBM)
9	CERT	IN1630SL	SRAM	—	ISM	8Kx8		0 4	double bit errors per data byte	IPN	No LU>72 Falguere [CERT], RADECS91, p479
9	ESA	MARS94 Flight Part	SRAM	CMOS Process S06A	MCN	32Kx8	~1 5	—	5	BNL	No LU>85 Harboe-Sorensen, RADECS93 preprint
9	CNES	MT5C1001	SRAM	CMOS	MCN	1Mx1	<0.3	0 5	40 to 70 (pattern dependent)	IPN	Ecoffet et al, IEEE93 Workshop Proton data exists Date Code 0133
9	MMs	MT5C1008	SRAM		MCN	128Kx8	—	—	—	GANIL	SHE (Single Hard Error] LET(th)=-50; 1E-3cm2 Poivey, IEEE-NS, 2235 (1994)
9	CERT	MT5C1008	SRAM		MCN	128Kx8	06	1 (worst "all 1 's")	Includes multiple errors	IPN	No LU >36 Falguere RADECS91, p 479
9	CNES	MT5C1008	SRAM	CMOS	MCN	128Kx8	<1 7	1 8	2510 150 (pattern dependent)	IPN	Ecoffet et al, IEEE93 & IEEE92 Workshop Proton data exists Date Code 9125
9	CNES	MT5C1008	SRAM	CMOS/epi LCRP [Ref 1]	MCN	128Kx8	<1 7, <7 @ 10%	2E-3	029 checkered address	IPN	Engr sample LCRP=low current resistor process Ecoffet 928 Workshop 93
9	A	MT5C1008	SRAM	CMOS/epi LCRP?	MCN	128Kx8	4 0 70% sat	2E-3	Single-word multiple upsets [SMUs]	88-In	No Lu.1o? Koga, IEEE93 Low cross section implies low current devices
9	MMS	MT5C1008C	SRAM	CMOS/bulk	MCN	128Kx8	—	—	—	GANIL	LU=75, 4E-4cm2, hard errors Dufour IEEE92; Poivey IEEE 94
9	CNES	MT5C1009	SRAM	Dale Code "ES"	MCN	128Kx8	<! 7	—	0.01 to 1 2 (pattern dependent)	IPN	Ecoffet et al IEEE93 Workshop Date Code "ES"
9	J	MT5C2568	SRAM	CMOS/epi (0 65 micron feature)	MCN	32Kx8	<1 4	006 & 04 (Remarks)	—	BNL	No LU >72 12/93 Cross section discrepancy needs resolution
9	J	MT5C2568-35	SRAM	CMOS/epi [suffix=read/write(ns)]	MCN	32Kx8	<14	003 [worst "all 1's"]	—	BNL	No LU >72 12/93 Same as next, except for giant error clusters d version -70
9	J	MT5C2568-70	SRAM	CMOS/epi [suffix=read/write(ns)]	MCN	32Kx8	<1 4	003 [worst "all 1's"]	—	BNL	No LU >72 12/93 Giant 32K error clusters at LET>26
9	ESA	MT5C2568C	SRAM	CMOS	MCN	32Kx8	<1 7	—	150	IPN	No LU >40 See later technology Harboe-Sorensen, RADECS93, p 490
9	CERT	MT5C2568C	SRAM		MCN	32Kx8	1	035	—	IPN	No LU >72 Falguere RADECS91, p 479
9	J	MSM8128K	SRAM	CMOS?	MOC	128Kx8	2 6	4E-3 (LET=26)	—	BNL	LU(th)=26 Dec 13, 1993
9	J	MSM8128KL	SRAM	CMOS	MOC	128Kx8	28	4E-3 (LET=26)	—	BNL	LU(th)=26 Dec 13, 1993 No difference between -K and -KL versions
9	ESA	MHS65162	SRAM	CMOS/epi	MTA	2Kx8	—	1 2E-2 (LET=20)	70 (LET=20)	GSI Microprobe	No LU> 20 Metzger et al, RADECS93
9	ESA	MHS65162	SRAM	CMOS/epi (10 micron)	MTA	2Kx8	4	3E-2 (LET=35)	—	GSI SIS	No LU>35 Dreute, RADECS9 ! .493 High vs lower energy comparison
9	CERT	HM65641	SRAM		MTA	8Kx8	4	0 2	—	IPN	No LU>72 Falguere, RADECS91, p 479
9	CNES	HM65656	SRAM	SCMOS/epi [high performance]	MTA	32Kx8	17	01	300	IPN	Ecoffet et al, IEEE93 preprint Proton data exists Date Code ES
9	EsA	MHS65664	SRAM	CMOS/epi [5 microns]	MTA	8Kx8	<10	! 2E-2	—	GSI SIS	No LU>35 Dreute et al, RADECS93
9	CERT	HM65664	SRAM	—	MTA	8Kx8	5	0.4	—	IPN	No LU>55 Falguere, RADECS91 p 479
9	CNES	D431000	SRAM	—	NEC	128Kx8	<3	—	Double hits	IPN	Ecoffet et al, IEEE93 Workshop Proton data exists Date Code 9137
9	CNES	04325.5	SRAM	—	NEC	32Kx8	<3	—	Double hits	IPN	Ecoffet et al, IEEE93 Workshop Proton data exists Date Code 9035
9	A	UPD43256A	SRAM	CMOS/NMOS	NEC	32Kx8	3	0 4	—	P#.in	No latchup March, 90
9	CNE S	CXK581000	SRAM	DC 9352	SNY	128Kx8	<17		0 7 to 7 (pattern dependent)	IPN	Ecoffet et al, IEEE93 preprint Proton data exists
9	J	CXK581000P-10LL	SRAM	CMOS/NMOS	SNY	128Kx8	14	018	suggests multiple errors	BNL	LU(th) between 15 & 38 Mar '93
9	CNES	CXK581001	SRAM	DC 9150/9151	SNY	128Kx8	<17	—	D 2 to 4 (pattern dependent)	IPN	Ecoffet et al, IEEE93 preprint Proton data exists
9	CNES	CXK58257	SRAM	—	SNY	32Kx8	<3	—	—	IPN	Ecoffet et ❑ I, IEEE93 preprint Proton data exists
9	MMS	SMJ44C251	SRAM (Video)	CMOS- 1 micron	TIX	256Kx4	0 5	—	! 20	MMS/GANIL	No LU>46 Beaucour, IEEE93 Workship, 7/93
9	IBM	IMS16-1EPI	SRAM	CMOS/epi	TMS [1]	64Kx1	3	0 3		88-in	No LU>60 T Scott 6/88 Proton data exists [1]= SGS Thomson
9	R	UT87164	SRAM	CMOS "prototype flow"	UTM	6K.6	>37	No upset	No upset	BNL	No LU >37 DC 9320 Bob Ferdon 7/10/93
10	GDO	MB8116400-60PJ	DRAM	CMOS	FUJ	4Mx4	<1 4	3 5		BNL	No LU>80 SEFI d LET-50 LaBel test 5/94
10	CNES	01 G9274	DRAM	Date Code ES	IBM	1Mx4	2 5	—	24	IPN	No LU Ecoffet et d IEEE93 Proton data exists
10	J/Loral	LUNA-C DD3	DRAM	CMOS/epi with ECC-- off	IBM	4Mx4	4 @ 3.14V	—	2	BNL	No LU >12003 42V T Scott, Loral Internal Rept #94 Gw3 008 (8/31/94)
10	CNES/ALC	LUNA-C	DRAM	CMOS/epi with ECC.. off or on	IBM	4Mx4	~3 @ 3 6V	~0 2 ECC off; 3E-3 on	—	BNL.S IPN	No LU> 120 Row & column errors unaffected by ECC Calvel IEEE94
10	CNES/ALC	LUNA-E	DRAM	CMOS/epi without ECC	IBM	4Mx4	~30 5V	~0 1	—	BNL 6 IPN	No LU>1 20 Row & column errors cross sections Compare above Calvel, IEEE 94
10	ESA	MT4C4001JC	DRAM	engr sample-shrunk 06rn,c line	MCN	1Mx4	~1 5	—	40 to 80	IPN	NO LU>120 DC 9244 Process D15B Harboe Sorensen RADECS93 p 490
10	CNES	MT4C4001	DRAM	DC 9109 & 9248	MCN	1Mx4	<0 4 to <1 7	—	5010150	IPN	No LU Ecoffet IEEE93 Workshop Stuck bits Proton data exist
10	GDO	MT4CM4B1DW	DRAM	CMOS	MCN	4Mx4	<1 4	LU obscures it	—	BNL	LU 12 to 26, 2E 4cm2 LaBel Test 5/94
10	J/TRW	—	DRAM	—	OKI	4M	<1	—	-50	BNL/88in	No LU>60 SEFI LET(th)= 16, 700 sq mic [F/F model] G Swift 94 SEU Symp
10	GDD	KM44C4000AJ-7	DRAM	CMOS	SAM	4Mx4	<1 46	—	17	BNL	No LU>110 Stuck bits & SEFI at LET>60 DC 408Y LaBel 7/94
10	IBM	SMJ27C128 25	DRAM	CMOS	TIX	16Kx8	Rates given	—	—	BNL	The data here were taken as a subset of the TIX SM320F15 DS P 5/93
10	IBM	44400	DRAM		TIX	1Mx4	—	—		BNL	No LU Soft error data exist Proton upset data exist T Scott, 990
10	CNES	SMJ44100	DRAM	Date Code ES	TIX	4Mx1	<0 4	—	>24	IPN	No LU Ecoffet et al IEEE93 Proton data exists SEU, preceding entry