Assembly Reliability of Ball Grid Array and Chip Scale Packages for High Reliability Applications

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Abstract

Different aspects of advanced surface mount package technology have been investigated for aerospace applications. Three key areas included the assembly reliability of conventional Surface Mount, Ball Grid Arrays (BGAs), and (Chip Scale Packages.

Reliability of BGAs was assessed as part of a consortium effort led by the Jet Propulsion Laboratory. Nearly 200 test vehicles, each with four packages, were assembled and tested using an experiment design. The most critical variables incorporated in the experiment were package type, board material, surface finish, solder volume, and environmental condition. The BGA test vehicles were subjected to thermal and dynamic environments representative of aerospace applications. The test vehicles were monitored continuously to detect electrical failure and their failure mechanisms were characterized.

A Microtype BGA consortium with imius[ry-wide. support was also organized to address technical issues regarding the interplay of package type, 1/() counts, PWB materials, and the manufacturing variables on quality and reliability of board level assembly. This paper will present the most current thermal cycling test results (>4,000 cycles) for ceramic and plastic BGA packages as well as their failure mechanisms. The bored level reliability of (Xl) assembly will also be reviewed and projected for a specific environmental condition.

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1. MINITURIZATION TRENDS

In surface mount technology (SMT), electronic packages are mounted and terminated dire'ctly onto the Printed Wiring Board (PWB) surface rather than inserting the leads into plated tbrougb-boles (PTH s). '1'here are several surface mount package styles, both active and passive. Active devices are divided into those with terminations of leads on the periphery of the component, two or tour sides, or those with terminations (either pads or solder bumps) over much of the bottom of the component. Peripheral Array Packages (l'Al') have less potential for significant size reduction with increased I/O counts compared to Area Array Packages (AAPs). The Ball Grid Arrays (BGAs) from the latter category are now the mainstay alternative to PAPs.

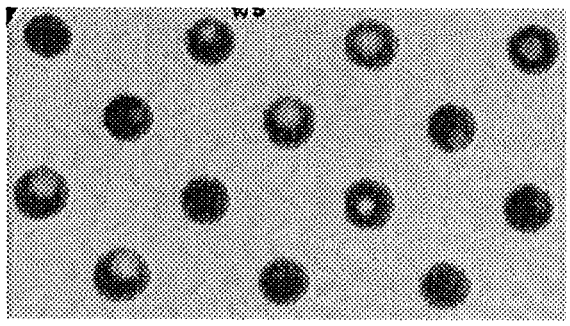
For example, the CSP version of the two sided PAP is the Lead-On-Chip (1 .OC) package and the versions for AAPs are micro- (or mini-) BGA packages generally with eutectic solder balls.

Another level of miniaturization is accomplished by directly attaching the bare die to the PWB. The direct Flip Chip On Board (FCOB) is the ultimate miniaturization level achieving nearly 70% efficient use of the area of the dic ratio to the PWB's footprint. In FCOB, solder bumps are permanently attached to the face of bare die, and the flip side is mounted on the PWB. In Chip-On-Board, with about 50% usc of area efficiency, the pads of the wire bonded die are used for second level wire bonding onto the PWB.

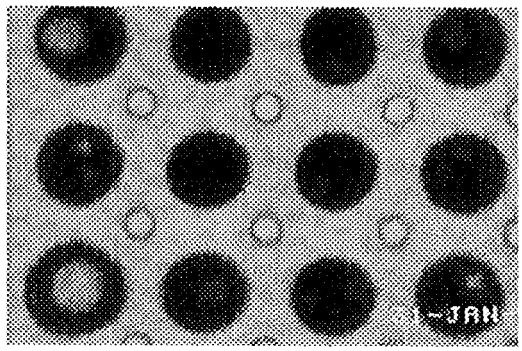
1- WHY BGA

BGA is an important technology for utilizing higher pin counts, without the attendant handling and processing problems of the peripheral leaded packages. They are also robust in processing because of their higher pitch (0.0S0 inch typical), better lead rigidity, and self-:lligllmcl]t characteristics during reflow processing.

BGAs' solder joints cannot be inspected and reworked using conventional methods and are not well characterized for multiple double sided assembly processing methods. In high reliability SMT assembly applications, e.g. space and defense, the ability to inspect the solder joints visually has

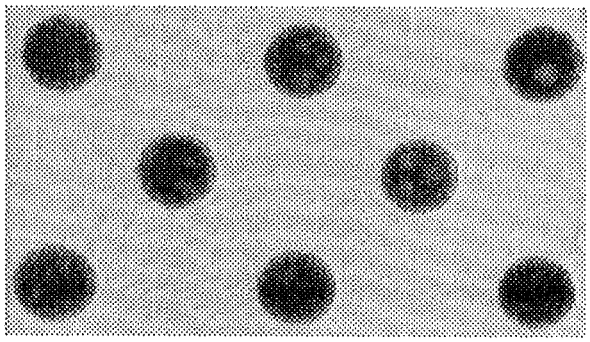


a) Excessive Voids in PBGA 313

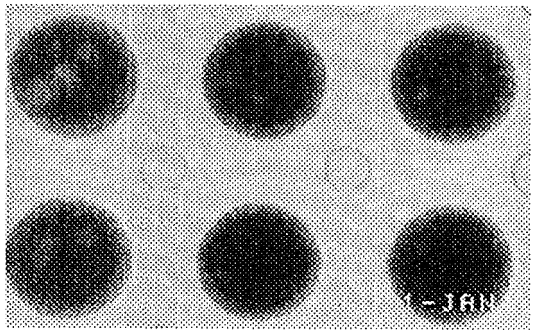


b) Excessive Voids in SBGA 352

Figure 1 Excessive Voids for Water Soluble Paste with an *RMA Reflow* Profile



a) Reduced Voids in 313 PBGA



b) Reduced Voids in 352 SPBGA

Figure 2 Voids for Water Soluble Paste with a *Water Soluble Reflow* Profile

Two test vehicles were assembled:

- Type 1, ceramic and plastic BGA packages with nearly 300 1/os
- Type 2, ceramic and plastic BGA packages with nearly 600 1/os. Also utilized were a 256 leaded and a 256 plastic BGA package for evaluating and directly comparing manufacturing robustness and reliability.
- Assemblies with water soluble flux were cleaned in an 1 'lectrovert I 1500. '1'hose with RMAs were cleaned used Isopropyl Alcohol (IPA) and a ***5940*** saponifier.
- All fine pitch QFPs had to be reworked for bridges.

4- BGA THERMAL CYCLING

Two significantl y different thermal cycle profiles were used at two facilities. The cycle A condition ranged -30 to 100"('and had increase/decrease heat ing rate of 2°C and dwelt of about 20 minutes at the high temperature to assure near complete creeping. The duration of each cycle was 82 minutes.

The cycle B condition ranged -55 to 125°C. It could be also considered a thermal shock since it used a three regions chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear and varied between 10 to 15 °C/min. with dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes. BGA test vehicles were continuously monitored through a LabView system at both facilities.

The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally once the first interruption was observed, [here were many additional interruptions within 10% of the cycle life. In several instances, a few non-consecutive early interruptions were not followed by additional interruptions till significantly later stages of cycling. This was found more with plastic packages as evidenced from 1 'igur3.

In 1 'igure 3, the total number of electrical interruptions (daisy chain opens) are plotted vs number of cycles. For ceramic BGAs, the slope or rate of interruption detection were approximately constant and were the same whereas this was not the case for the plastic BGAs. For a PBGA with 313 I/Os, the first interruption occured at 913 cycles with no additional interruptions till about 3,000 cycles. Further erratic interruptions were occured between 3,000 and 3,700 cycles, followed with a linear interruptions with the Slope the same as CBGAs. Another PBGA showed interruptions at 3130 cycles, and become open after about 300" additional cycles.

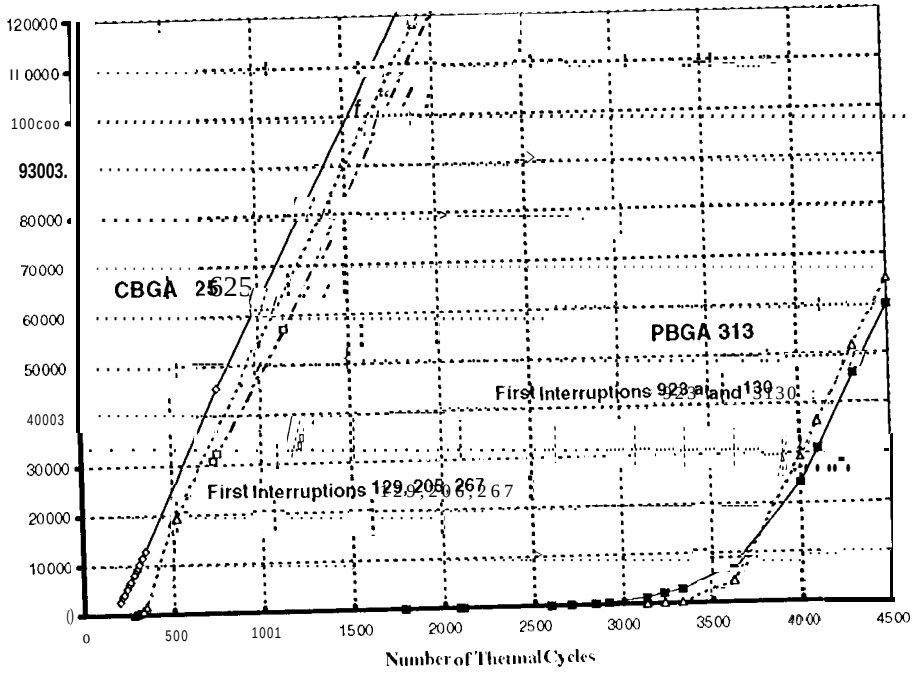


Figure 3 Number of Electrical Interruptions Detected with Thermal Cycles for Ceramic and Plastic BGAs

Damage Monitoring

For conventional SMT solder joints, the pass/fail criteria for high reliability applications relies on visual inspection at 10x to 50x magnifications. For BGA, only edge balls, those not blocked by other components, were visually inspected. A series of single assemblies cut from the test vehicles were used for both visual and SEM inspection to better define visual criteria for acceptance of solder joints as well as to monitor damage progress under different cycling environments.

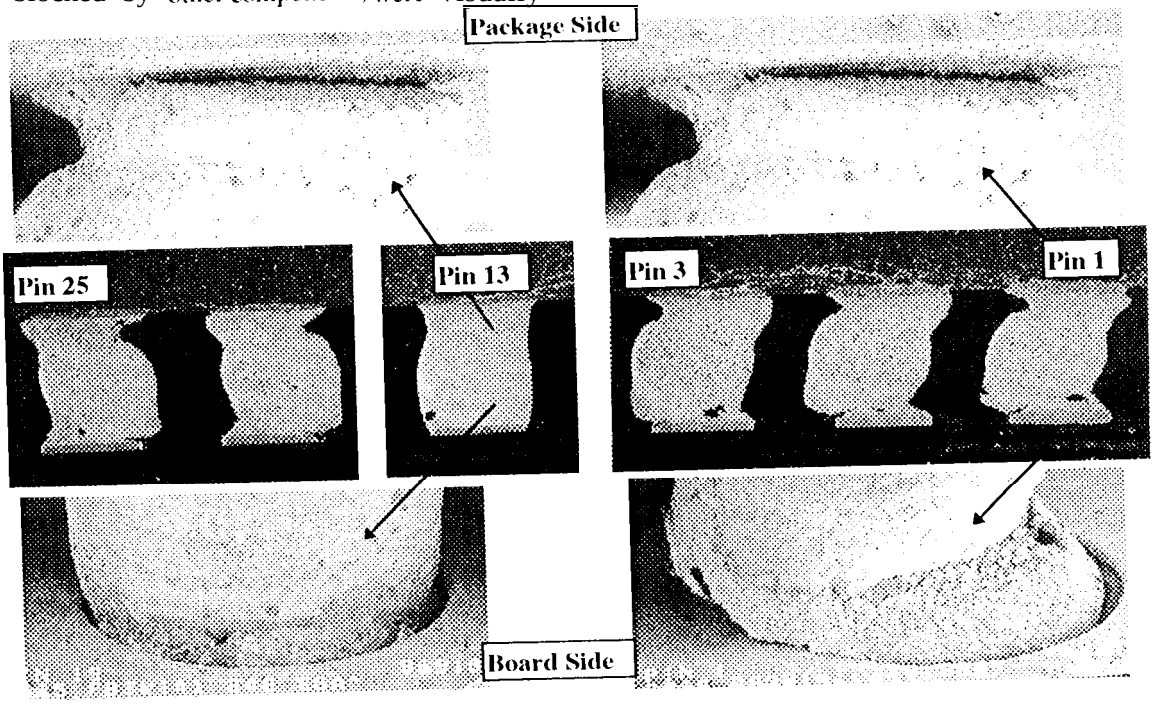


Figure 4 SEM and Cross-section photos for CBGA 625 after 348 cycles (-30°C to 100"C)

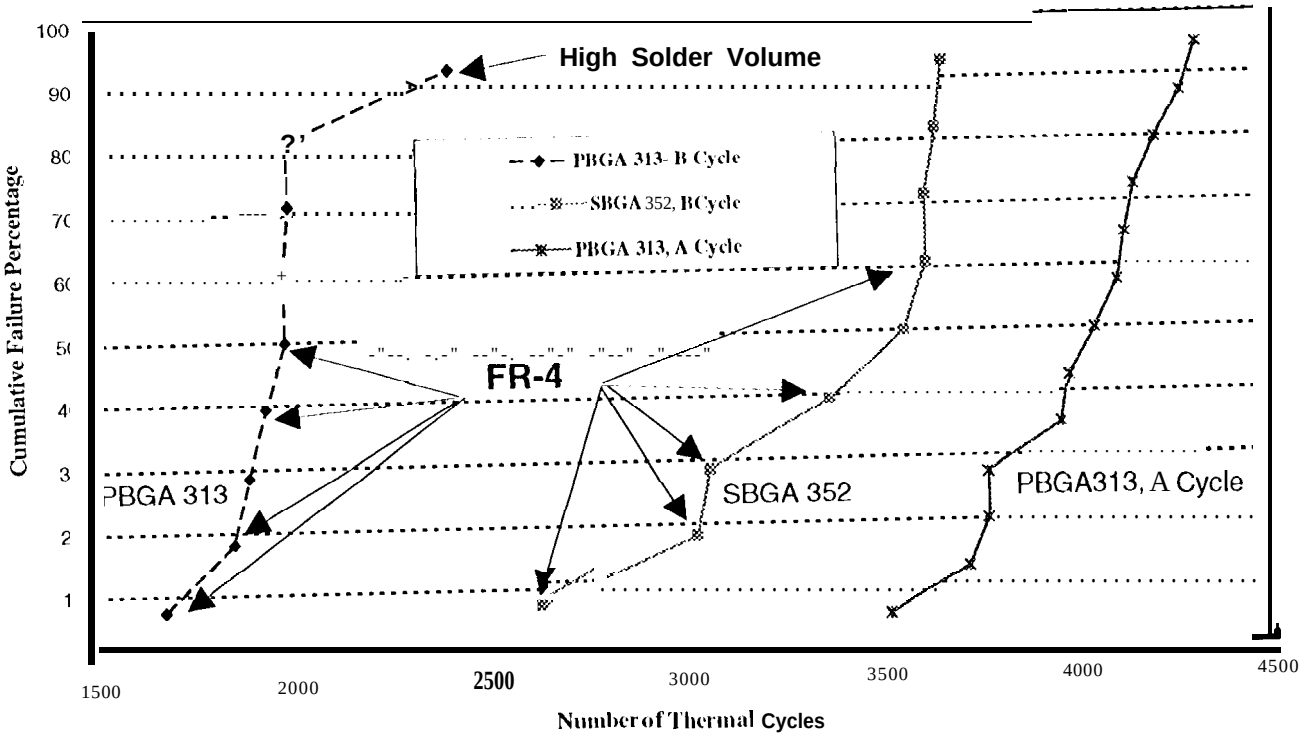


Figure 5 Cycles to Failure for PBGA 313 & SBGA 352 Assemblies (-55°C **to 125°C, A) & (-30°C to 100"C)**

Figure 4 shows a representative SEM and cross-sectional micrographs for a CBGA 625 after 348 cycles of A conditions. Cross-section photos are for the perimeter balls, two corners and a center ball. SEM photos for package and board sides of a corner (maximum Distance to Neutral Point(DNP)) and the edge center ball are included.

For the B cycles ceramic packages failed at the package interface with signs of significant creeping and solder grain growth[3]. The board side solder creeping and cracking were much milder.

Thermal Cycling Results

Figure 5 shows cycles to first failure for PBGA 313 and SBGA 352 subjected m B cycling for assemblies on polyimide and FR-4 PWBs. The most current PBGA 313 assemblies that failed under cycle A conditions are also included in the plots for comparison. These assemblies include those reflowed with low, standard, and high solder paste levels.

The cycles to failure were ranked from low to high and failure distribution percentiles were approximated using median plotting position, $F_i = (i-0.3)/(n+0.4)$. Weibull parameters will be generated when all failure data are gathered.

5- CHIP SCALE PACKAGES

Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and are now at the stage Ball Grid Arrays (BGAs) were about two years ago. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. CSPs are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Many manufacturers now refer to CSPs as packages that are the miniaturized version of their previous generation. Two concepts of CSPs are shown in Figure 1. Packaging accomplishes many purposes, including the following:

- Provides solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes
- Redistributes the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. The small sizes of CSPs do not permit significant redistribution and the current cost effective PWB fabrication limits full adoption of the technology, especially for high 1/0 counts.
- Protects the die from physical and alpha radiation damages, and provides a vehicle for thermal dissipation
- Eases die functionality testing.

CSPs generally have been categorized based on their fundamental structures . These are:

- Interposer packages with either flex or rigid substrate
- Wafer level molding and assembly redistribution
- Lead On Chip (LOC) packages.

6- CSP Assembly Reliability

Currently, most data were generated for package qualifications by manufacturers, with very limited published information available on assembly reliability. These data are of limited value to the end user since often they have been collected under significantly different manufacturing and environmental conditions or for packages with different pin counts.

Failure at the board level could be caused by either the failure of the package itself or the package to board connection. The latter could be caused by the intrinsic wear-out mechanisms or by hostile environmental factors. The thermo-mechanical wear (creep) of solder joints is the cause of failure for most CSP assemblies. Failure of a solder joint can be caused by mechanical stresses in a non-uniform thermal expansion and/or by contraction of different materials in the assembly. To achieve the least damage to solder joints, thermal mismatch between the die and board should be minimized either by package optimization or by appropriate board material selection to closely match coefficient of thermal expansion (CTE) of package. Only a few of the CSP packages have been designed to alleviate damage due to the thermal expansion of package/board mismatches.

Literature Data on CSP Assembly Reliability

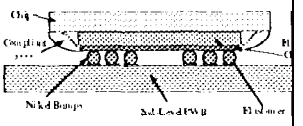
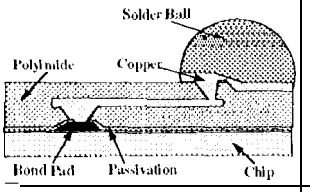
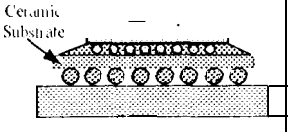
Table 2 lists the assembly reliability for flex or rigid interposers, and wafer level packages. Aspects of cycling conditions with their failure mechanisms are summarized in the following:

- CTE absorbed CSP: Thermal cycling test results for a CTE-mismatched relieved package are shown in the Table 1. This package uses TAB-like IC interconnects, a resilient elastomeric interposer, and eutectic solder balls. The resilient interposer in conjunction with the springiness of TAB interconnection reduce thermal expansion differences between the chip (CTE 2-3 ppm/°C) and PWB (CTE for FR-4 ~15 ppm/°C). This package has been shown to be reliable, robust, with no requirement for underfilling. Thermal cycling/shock data given in the Table were for daisy chain packages on FR-4 and were performed from the liquid nitrogen temperature (-196°C) to hot oil (160°C). Because of the low strain state of solder joints, fatigue failure mechanisms of solder joints were not observed and failures shifted to the heel of TAB interconnection with high mismatched stress levels. Significant improvement was observed when ductile gold leads were used. The gold version showed no failure up to 2000 cycles in the range of -65°C to 150°C. The thermal cycling screening test results associated with assembly exposures to extremely low (stress conditions) and high temperatures (strain conditions) are not realistic and therefore their failure mechanisms may not be representative of field failures. One such failure, due to extreme high temperature exposure, is the chambering and deformation of FR-4 close to its glass transition temperature (Tg). The PWB materials will show severe damage if cycling temperature becomes close or exceeds their glass transition temperatures, the temperature that polymer materials started to become soft. Indeed, it was observed that FR-4 plated through holes had massive barrel cracking failure for -65°C to 150°C temperature cycling range.
- Wafer packages with extreme CTE mismatch: Thermal cycling test results for assembly of a wafer redistributed package is shown in Table 1. In this package, a thin film metal/polymer redistributes the location of the solder bumps over the chip to make these compatible with the surface mount footprint. The height of the package type increases by the thickness of the metal polymer layer from the bare chip. This additional layer will not generally absorb the CTE mismatch between the chip and board and therefore the assembly reliability of these package is expected to be very similar to C4 assemblies. Without underfill materials, the assembled package failed less than 40 cycles when subjected to thermal cycling between 0°C and 100°C. For these types of packages, underfilling is usually required to achieve an acceptable level of assembly reliability. The underfilled assemblies did not fail up to 2,000 cycles.
- Ceramic packages with rigid interposer: The non-wafer level ceramic packages have shown reasonable assembly reliability with no underfilling. Thermal cycling results for a ceramic package on FR-4 is also included in the Table 1. The ceramic CSP uses the same design rules as multilayer ceramic (MLC) with the first level interconnection choices of thermal compression and gold stud bump, solder flip chip, and wire bond. The strength, rigidity, coplanarity, and chamber of package are excellent. The package assembly on a 0.6 mm low Tg FR-4 failed at about 600 thermal cycles between -40°C to 125°C. Cycles to failure increased to more than 900 cycles when PWB thickness increased to 1.6 mm. Thicker FR-4 is expected to show better rigidity when exposed to 125°C, temperature close to the low Tg FR-4 polymer used for this study.

Assembly Reliability for Conventional Packages and Those Projected for CSPs

Reliability of conventional SM packages also have been investigated at JPL[4]. Cycles to failure test data points and their Weibull distributions for 28-, and 20-pin LCC, and 68-pin gull wing assemblies are shown in Figure 6. Thermal cycling ranged from -55°C to 100°C with 246 minute duration. The failure distribution percentiles were approximated using a median plotting position, Fi = (i-0.3)/(n+0.4). The two-parameter Weibull cumulative failure distribution was used to fit data.

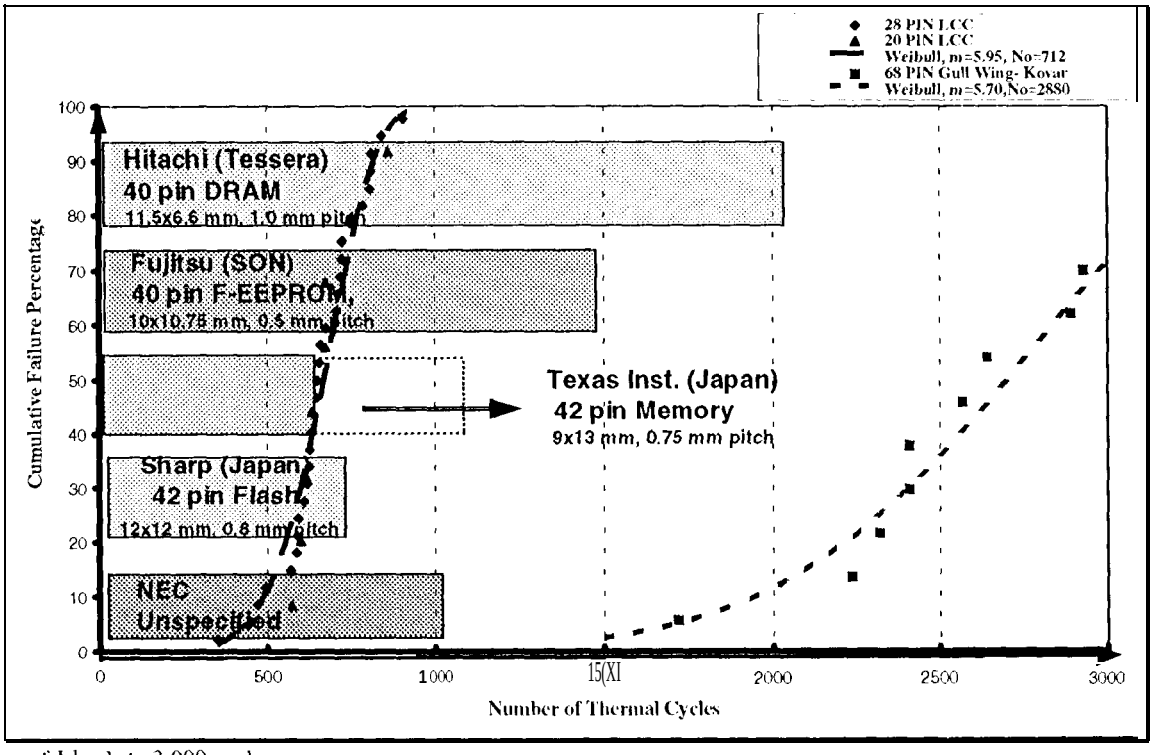
Table 2. Literature Data on CSP Assembly Reliability

Package Type Schematic (not to scale)	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References (comments)
Flex Interposer CTE matched 	-196°C<>160°C -65°C<>150°C	130 no underfill 1163 2000*	0/3 0/40 0/34	188 188	J. Fjelstad, T. DiStefano, B. Faraji, C. Mitchell, J. Kovac, "µBGA Packaging Technology for Integrated Circuits," *NEPCON East*, June 1995 T. DiStefano, J. Fjelstad, "Chip-scale Packaging meets future design needs," *Solid State Technology*," April 1996 * Gold bond ribbon. Ductile-copper bond ribbon survived 500 Cycle...
Wafer Level Redistribution 	0°C <>100°C (Thermal Shock)	>2000 underfill <40 no underfill	NA	266	R. Chanchani, et al, "miniBall Gird Array (mBGA) Assembly on MCM-L Boards," *Proceedings of Electronic Components and Technology Conference*, May 18-21, 1997
Ceramic CSP 	-40°C <>125°C	~600* no underfill, PWB 0.6 mm >900* no underfill, PWB 1.6 mm	NA	220	R. Ianzone, "Ceramic CSP: A Low Cost, Adaptive Interconnect, High Density Technology," *Proceedings of second International Conference on Chip Scale Packaging, CHIPCON '97*, Feb. 20-21, 1997 *Private Communication

- For **comparison,** projected cycles to failure for low count CSPs are also included. Results are those gathered from literature and projected based on a modified Coffin-Manson relationship. Board reliabilities of most CSP packages are comparable or better than their LCC counterparts. These packages, however, are not as robust as leaded packages including gull wing and J-leads (data for J-leads are not shown in Figure 6 since there were no joint failures to 3,000 cycles).

7- SYSTEMATIC APPROACH TO ASSESS CSP BOARD RELIABILITY

Board reliability information is a key element in facilitating CSPs implementation in commercial and especially in high reliability applications. For wider applications of this technology, the potential user will need design reliability data since often they have no resources, time, or ability to perform complex environmental characterizations. To help to build the infrastructure in these areas, JPL has formed a consortium with the objectives of addressing many technical issues regarding the interplay of package type, I/O counts, PWB materials, surface finish, and manufacturing variables for the quality and reliability of assembly packages. The JPL-led microtypeBGA consortium is now building its first test vehicle with sixteen packages from eleven manufacturers with I/Os ranging from 12 to 540.



*No failure of J-leads to 3,000 cycles

Figure 6. Projected Cycles to failures for Low Pin Count CSP Assemblies and Cumulative Failure Distributions for Conventional SM Package Assemblies Tested at.] 1'1. (-55°C to 1(M)"(;)

8- CONCLUSIONS

BGA Packages and Assembly Reliability

- Planarity levels dependent on package types, but irrespective of package types decrease as the size decreased.
- Ceramic packages showed lower warpages and were more coplanar than (heir PBGA counterparts. Numerous ceramic packages had tilted solder balls.
- Solder ball planarities were significantly higher for plastic than for ceramic packages. A few PBGAs showed unexpectedly higher values above their norm distribution. PBGAs, however, are more robust and the large planarity values might not be as detrimental to their solder joint reliability as those for ceramics. Some planarity differences among the PBGA balls were accommodated by their collapses during the reflow process, This is not the Gist for CBGAs where high melt solder balls remained intact during reflow. The solder ball diameter controls the stand-off height which is a key factor in solder joint reliability.
- 3D laser scanning is excellent for characterization of package dimensions, but possibly not for solder ball measurement.
- The BGA assembly void levels were the same as those generally observed by industry. As expected, BGAs were robust in assembly compared to the 256 fine pitch, 0.4 mm QFPs. All QFPs showed bridging to some degree and had to be reworked.
- RMA and water soluble reflow profiles evaluated in this study were significantly different and they were optimized separately for the applications. Large number of rather smaller and sporadic voids were generated when an RMA reflow profile for a water soluble solder paste was used.
- As expected, ceramic packages failed much earlier than their plastic counterparts because of their much larger CTE mismatch on FR-4/Polyimide boards. Cycles to electrical failure depended on many parameters including cycling temperature range and package size (I/O).
- Ceramic packages with 625 I/Os were first to show signs of failure among the ceramic (CBGA 361) and plastic packages (SBGA 560, SBGA 352, OMPAC 352, and PBGA 256) when cycled to different temperature ranges.
- Joint failure mechanisms for assemblies exposed to two cycling ranges at two facilities were different. Ceramic assemblies cycled in the range of -30°C to 100°C showed cracking initially at both interconnections with final separation generally from the board side through the eutectic solder. The board side joint showed signs of pin hole formation prior to cracking and complete joint failure. This failure mechanism is similar to

those reported in literature for 0°C m 1 00°C thermal Cycles.

- Ceramic and plastic BGAs showed different failure mechanisms as evidenced from the total number of electrical interruptions with cycles. For CBGAs, the first electrical interruption (open) followed by consecutive additional interruptions. This was not the case for PBGAs where the first interruption was not followed by additional interruptins till much higher number of cycles.
- The PBGAs with 313 1/(), depopulated full arrays, were first among the PBGAs to fail with both cycling ranges. It has been well established that this configuration, with solder balls under the die, is not optimum from a reliability point of view.
- Solder volume is generally considered to have negligible effect on plastic package assembly reliability. One PBGA 313 package that was assembled with a high solder paste volume under cycle B exposure showed the highest number of cycles to failure. This will be assessed when data for cycle A become available.
- The 352 SBGA with no solder balls under the die showed much higher cycles to failure than the PBGA 313 when subjected to cycle B conditions.
- For cycle B conditions, plastic package assemblies (PBGA 313 and SBGA 352 on polyimide) generally failed at a higher number of cycles than those on FR-4.

CSP Assembly Reliability

- The board level reliabilities of most (X1' packages are comparable or better than their LCC with similar 1/() counts. These packages, however, are not as robust as leaded packages including gull wing and J-leads.
- Limited CSP assembly reliability data are being generated by manufactures and end users. Systematic approaches to understand contributions of variables including package types, board materials and surface finishes, manufacturing parameters, and testing methodologies are non existence. The JPL-led consortium is formed to address systematically many of these issues. Understanding the overall philosophy of testing to meet system requirements as welt as detecting new failure mechanisms associated with these miniaturized packages are key in collecting meaningful test results.

9- REFERENCES

1. Ghaffarian, R. "Area Array Technology Evaluation for Space and Military Applications", The 1996 International Flip Chip, Ball Grid Array, TAB and Advanced Packaging Symposium Proceedings, Feb. 13-16, 1996.

2. Ghaffarian, R. "CBGA/PBGA Package Planarity and Assembly Reliability", The 1997 International Flip Chip, Ball Grid Array, TAB and Advanced Packaging Symposium Proceedings, Feb. 17-19, 1997.

3. Ghaffarian, R., N. Kim, "Ball Grid Reliability Assessment for Aerospace Applications," 30th International Symposium .. 011 _ Microelectronics, Philadelphia, Oct. 12-16, 1997

4. Ghaffarian,R, "The Interplay of Solder Joint Quality and Reliability for Leaded and Leadless Components," Ninth Annual Soldering Technology for Electronic Packaging Symposium, Oct. 21-25, 1996, Binghamton, NY

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