

# ADVANCED INTERCONNECT ROADMAP FOR SPACE APPLICATIONS

LISSA GALBRAITH, Ph.D.  
JET PROPULSION LABORATORY  
CALIFORNIA INSTITUTE OF TECHNOLOGY  
PASADENA, CALIFORNIA

## Abstract

*A roadmap giving technology forecasts and recommendations for research direction for advanced electronic interconnection technology for space applications is presented. Advanced interconnection technology addresses the effective integration of several critical and complex electronic packages and technologies. The Roadmap introduces major technologies in use and the related strategic issues facing research in the field.*

## Keywords:

Interconnection, electronic packaging, ball grid arrays, area arrays, chip scale packages, printed wiring assembly, roadmap, technology forecasts

## INTRODUCTION

The NASA Code AE Parts and Packaging Functional Initiative Program addresses the effective integration of several critical and complex electronic packages and technologies. This Roadmap introduces major technologies in use and the related strategic issues facing the Program. Technology forecasts and recommendations for research direction are given with a focus on information insight and application. The National Roadmap Coordinating Committee, hosted by the National Electronics Manufacturing Initiative (NEMI), has facilitated an agreement among electronic industry organizations to standardize and integrate industry roadmaps. The roadmaps involved include the IPC Interconnection Substrate Roadmap, the NSIC Magnetic and Optical Storage Roadmap, the SIA Semiconductor Roadmap, the OIDA Optoelectronics and Optical Storage Roadmaps, and the USDC Display Roadmap, all of which are linked to NEMI's series of National Electronics Manufacturing Technology Roadmaps. The NEMI series has been surveyed for this paper.

Electronic packages are optimized to be low cost and portable, robust and high speed, efficient users of power, and of small size and low weight. Mass customization, encouraged by the recent rate increase of virtual enterprise creation, is driving manufacturing toward perfect products and highly flexible manufacturing, already an area of NASA expertise. Society as a whole needs NASA's extensive experience in this arena. NASA can help government develop the necessary processes for a knowledge-based economy. A glossary is provided for all the acronyms used in this paper.

## FORECASTS

There are several general forecasts evident at this time:

1. Merging of ultra-fine pitch, flip chip, and hybrid assembly techniques.
2. Increased use of multiple technologies in one package such as optoelectronics or MEMS.
3. Thinner substrates from improved liquid encapsulation methods.
4. New packaging materials meeting greater moisture resistance.
5. Underfill materials which are fast processing and curing, low stress, fine gap, and compatible with no-clean fluxes.
6. Reduced wicking process time for injection and vacuum methods.

Pick-and-place systems will now place chips and flip chip die on the same board. Dispensers will apply SMD epoxy and conductive silver epoxy in a single board design. The disciplines of ultra-fine-pitch, flip chip and hybrid circuit manufacturing will continue to move rapidly into the SMT arena. The major driving forces pushing BGA use are: low cost 64%, decreased size 49%, compatibility with equipment 25%, faster time to market 19%, and increased circuit speed 9%<sup>4</sup>. Two major directions for the SM industry include higher density systems (flip chip) and the increased use of multiple technologies in the same package, such as electronic devices with optoelectronics and/or MEMS. PBGA packages remain the highest volume of use in the BGA family, TBGA and CBGA applications are growing<sup>11</sup>.

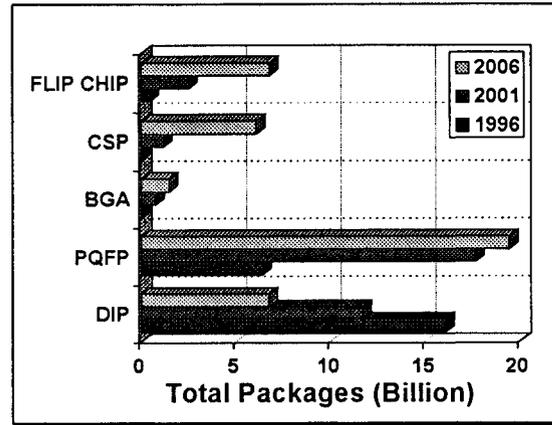
The major impetus for CSP use is the need for greater functionality in smaller board area. One year ago,

CSPs were primarily utilized in devices with less than 250 I/Os. High production CSPs are typically using flexible substrates such as TAB. Wafer-level CSP use is expected to increase, offering cost-savings at the wafer level<sup>11</sup>. Future directions for CSP development are expected to include<sup>8</sup>:

1. Thinner substrates from liquid encapsulation methods.
2. New packaging materials which can meet at least Level 3 moisture resistance and in many cases, Level 1.
3. PCB build-up or sequential processes development to satisfy high density interconnection requirements. Associated costs must be driven below \$2/in<sup>2</sup> before there will be wide acceptance.
4. Flip chip underfill materials attributes include fast processing and curing, low stress, fine gap, and compatibility with non-clean fluxes, however CSP technology needs even shorter process times for volume production. NASA benefits from such volume production research, even when applying the technology to very low volume builds. Anisotropic conductive films and pastes still in development have significantly higher costs than liquid underfill materials.
5. The wicking process time must be reduced. Forced wicking using injection or vacuum is under study.

Flip chip applications have increased moderately, with the Flip Chip Inside Package (FCIP) gaining popularity. The use of flip chip on board packages is expected to increase, but growth is limited by the need for low cost bumping, availability of cost effective substrates, better bare die testing, underfill time, and rework efficiency. Flip chip use is forecast to be in the FCIP arena, both CSP and BGA.

Projections regarding the use of through hole and surface mount IC packages significantly differ and the numbers depend on the marketing source. One projection from the BPA, UK, is shown below. Several trends are apparent.



Source: Adapted from BPA, SMI, 1997

Projection of Package Use (1996-2006)

The Dual In Line Package (DIP) had the most reduction in use, decreasing from 16 billion in 1996 to about 5 billion in ten years, i.e., about a one billion reduction per year. In contrast, the use of surface mountable packages including PQFPs (Plastic Quad Flat Packs) is projected to increase in the next decade. The increase is forecast to be from 7 to 18 billion within the first five years and will almost plateau with an increase of only two billion for another five years. Within ten years, the COB (Chip On Board), not shown in chart above is expected to increase from 5 billion to 13 billion.

The increase in the use of CSP and flip chip packages are expected to be about the same, projected to reach 6 billion by 2006. In contrast, the increase in BGAs for the same ten years is expected to be minimal, reaching a total use of only 1.5 billion. The projection for BGAs indicates that perhaps these packages were only an interim solution and were the stepping stone for the industry's wider acceptance of flip chip and chip scale packages. CSPs better meet the demands for denser and lighter attributes required for miniaturized applications.

Future NASA work in the MCM area will look at survivability and long life operation in extreme (both hot and cold) environments. These studies will need to address both the substrate and the various interconnects. This would enable the use of advanced MCMs in landers and rovers for various solar system exploration missions. As systems architectures are shrunk to fit in small packages, the interconnect between slices on stacked MCMs will deserve study. New interconnect technologies, including both elastomeric and distributed fiber contacts should be the focus of studies to determine the interconnection reliability, survivability, and life. The effect of shrinking geometries on electromagnetic interference and compatibility within and between modules will also need examination.

Flexible component mounting machines are becoming more accurate — to within  $\pm 25$  microns and lower, with the added ability to handle odd-shaped components. Flip chip assembly will require accuracies of  $\pm 5$  microns for reliable production<sup>2</sup>.

### **Research Recommendations**

Research recommendations for the various component types and for photonics processes are discussed above. Material and process research recommendations are given below.

NIST has identified four general areas of research emphasis in their Advanced Technology Program Microelectronics Manufacturing Infrastructure initiative:

1. Wafer technology
2. Semiconductor packaging
3. Very high density off-chip interconnects
4. Chip-to-board integration.

• **New underfill and glob-top encapsulant materials:**

1. New encapsulants which don't require high temperature curing cycles, yet which meet rigorous outgassing and adhesive requirements. Epoxies which can be cured at room temperature through the use of ultraviolet or visible light are of especial interest for glob-top applications.
2. New encapsulants should be investigated that can be easily removed for rework/replacement/repair of dice and/or substrates. Thermoplastic materials are strongly suggested for this application, which require the formation of temporary bonds during the manufacture and testing of the devices.

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3. New adhesives should be investigated that can be used for cryogenic applications.

• **New fluxes and solder pastes:**

1. New pastes for ultrafine pitch Quad Flat Packs (QFPs), Ball Grid Arrays (BGAs) and other area array packages, micro BGAs and other Chip Scale Packages (CSPs), and Direct Chip Attach (DCA)

processes.

2. Newer methods for cleaning fluxes and solder pastes, including water-based cleaning systems, newer solvents, as well as the use of nitrogen-atmosphere soldering to reduce the amount of cleaning required and also to reduce the formation of solder balls.
3. Fluxless solder attachment which eliminates the problems discussed earlier.

• **New conformal coating materials and methods for removing conformal coatings once applied:**

1. Develop the process of applying paralene coatings to PWAs and determine how to remove paralene efficiently. Investigate and specify the necessary capital equipment. This would obviate the entire Volatile Organic Compounds (VOC) issue regarding conformal coatings.
2. Investigate methods for removing conformal coatings from PWAs. The most promising method is a technique using CO<sub>2</sub> as an abrasive reducer.

• **Producing and metallizing small vias:**

1. New techniques for producing very small vias (microvias) should be examined, such as laser drilled, photoimaging, and plasma etching.
2. New techniques for metallizing the microvias should be examined.
3. The reliability of such microvias should be determined using thermal cycling, thermal shock, and other accelerated testing methods.

• **New technologies that are well-suited to solder deposition**

1. Wafer bumping for flip chip and optoelectronics packaging.
2. Via filling.
3. Three-dimensional printing.

• **New materials and processes for producing small form factor PWAs:**

1. Examine elastomeric and distributed fiber contact interconnects reliability.
2. Eliminate the use of solder paste, then no cleaning will be required.
3. If solder pastes are used, cleaning is a concern. Different methods must be investigated since it will prove increasingly difficult to clean under components with a large I/O count.
4. Testing. Board real estate will be at a premium on small form factor PWAs; it will be a challenge to design adequate test points without negating the guiding principle of this type of PWA.

5. Rework: finding a method to successfully remove the small form factor component without either damaging it or the PWB will prove challenging.

- **Mounting systems** with advanced vision capabilities able to handle a variety of packaging carrier formats. A figure showing the basic structure for Pluggable BGA (PLBGA) and Land Grid Array (LGA) is shown at the end of the text for this paper. These are two demount options which permit separate processing of the board and component, which eliminates CTE mismatch and facilitates field service. Field service is often not an option for space applications.

- **Design guidelines and process improvements are needed for direct chip attach:**

1. Design guidelines for COB passivation techniques.
2. Validated test regime for range of space flight environments.
3. Integration with design validation of chip scale packages, COB, and flip chip.
4. DCA manufacturing process control guidelines.
5. Cladding for DCA site preparation.

- Two major areas need to be pursued in MCM research:

1. Polymeric materials evaluation including:
  - \* High density deposited and thin film dielectric coatings
  - \* Low-K dielectrics for high frequency applications
  - \* Multiple dielectric/ceramics
  - \* Integrated thin film passive logic and thick film polymeric sensors.
2. Laminate versus ceramic substrate performance evaluation.

- **MEMS research suggestions are varied:**

1. Failure mechanisms as a function of design, materials, and mission length.
2. MEMS materials usage mission length and environment guidelines.
3. Critical points for inspections and process controls for mems manufacturing.
4. Non-invasive inspection and test methods for MEMS manufacturing and final products.

- **Reflow processes** for chip scale package mounting that are compatible with mixed assembly technology.

- **New cleaning chemistries and cleaning processes** for dense, small form factor PWAs containing components such as BGA, CSP, and/or DCA

- **Several aspects of testing:**

1. Improve test equipment capable of wafer level high performance electrical test.
2. Enhance wafer level burn-in.
3. Refine non-contact fault isolation testing for assemblies.
4. Develop the ESS test protocol(s) for dense, small form factor assemblies with complex components.
5. Determine the effects of miniaturization on electromagnetic interference and compatibility within and between modules

- **Rework/repair systems** with advanced vision capabilities to handle a variety of situations involving complex parts and small boards.

- Several research topics need emphasis in the **photonics** area:

1. Use of solid state laser, ultra-stable laser, and semiconductor laser.
2. Space-ready single-mode microwave fiber optic link qualification.
3. Frequency shifter qualification.
4. Integration and validation of optical/electronic back plane for electro-optic assemblies.
5. Evaluation of -80°C to +85°C range fiber optic cable.

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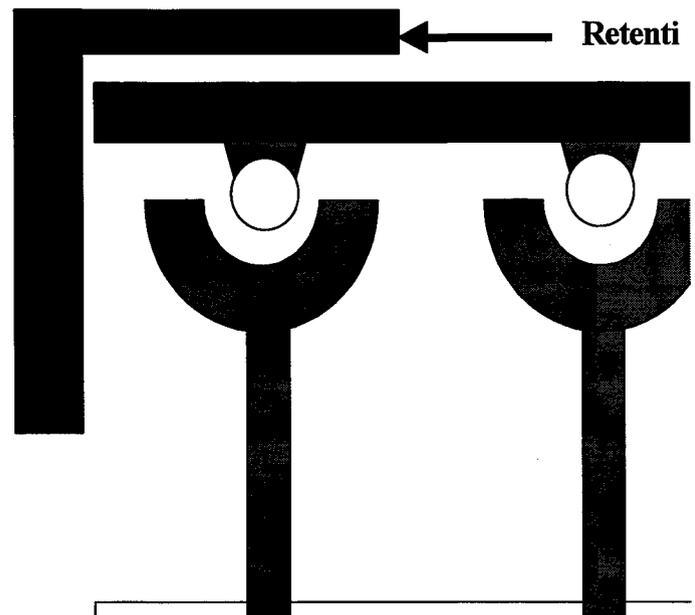
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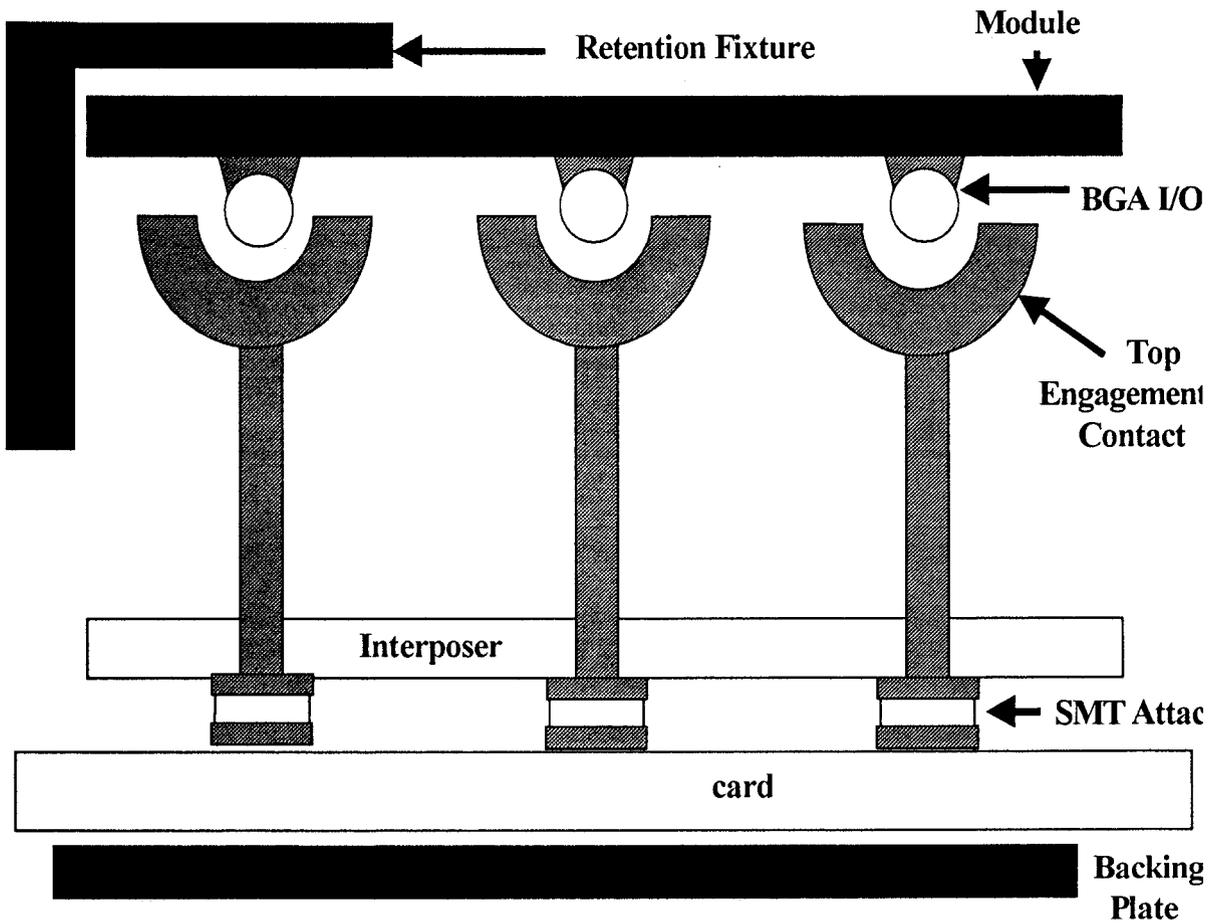
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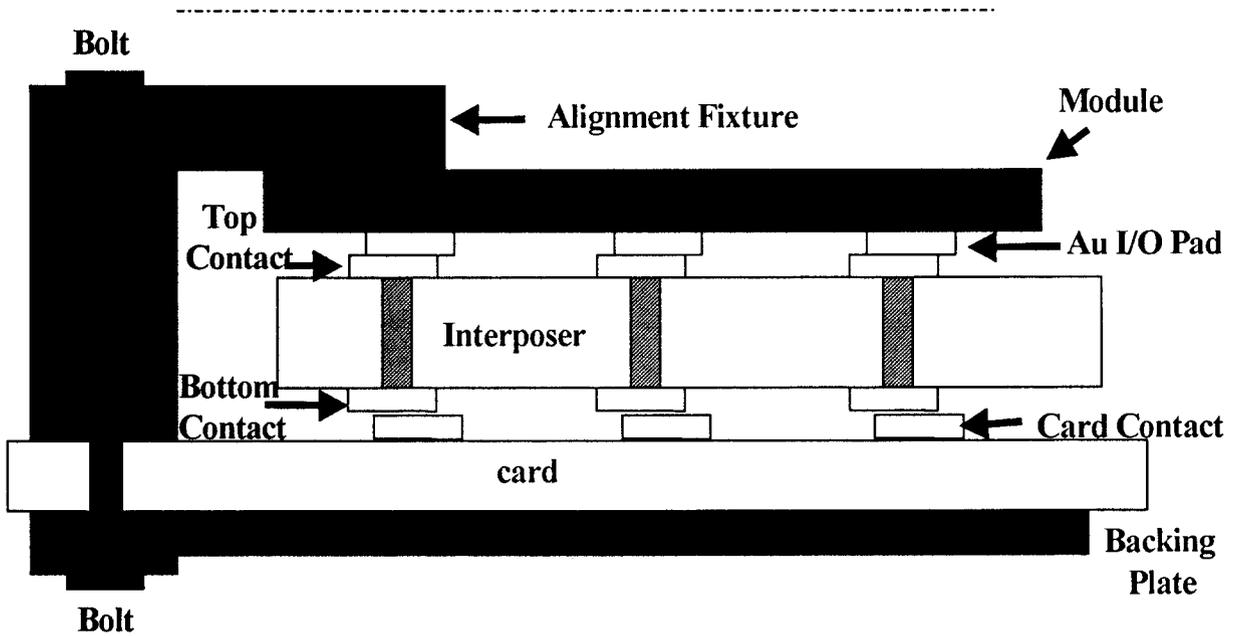
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**Pluggable Ball Grid Array (PLBGA)** [Puttlitz]



**Land Grid Array (LGA)** [Puttlitz]

## GLOSSARY

ANSI: American National Standards Institute  
A<sub>r</sub>: Aspect ratio  
ASIC: Application-Specific Integrated Circuits  
BGA: Ball Grid Array  
CBGA: Ceramic Ball Grid Array  
CCA: Circuit Card Assembly, aka PWA  
CCGA: Ceramic Column Grid Array  
COB: Chip on Board  
CSP: Chip Scale Package  
DBGGA: Dimpled Ball Grid Array  
DCA: Direct Chip Attach  
DSP: Digital Signal Process  
EIA: Electronics Industries Association  
EMPF: Electronics Manufacturing Productivity Facility  
FCIP: Flip Chip Inside Package  
FPGA: Field-Programmable Gate Array  
HASL: Hot Air Solder Leveling  
HFC: Hydrofluorocarbon  
ICT: In Circuit Testing  
IEC: International Engineering Consortium  
ILB: Inner Lead Bonding  
IMAPS: International Microelectronics and Packaging Society  
I/O: input/output, a lead  
IPC: Institute for Interconnecting and Packaging Electronic Circuits  
ITRI: Interconnection Technology Research Institute  
KGD: Known Good Die  
LGA: Land Grid Array  
LOC: Lead On Chip  
LS: Low Solids  
ManTech: Air Force Manufacturing Technology Program  
MBU: Multilayer BuildUp  
MCC: Microelectronics and Computer Technology Corporation  
MCM: MultiChip Module  
MCM-C: MultiChip Module with cofired ceramic substrate  
MCM-D: MultiChip Module with deposited thin film  
MCM-L: Laminate MultiChip Module  
MEMS: Micro-Electromechanical System  
NEMI: National Electronics Manufacturing Initiative  
OSP: Organic Solderability Preservative  
PASS: Photonics Applications for Small Spacecraft  
PBGA: Plastic Ball Grid Array  
PCB: Printed Circuit Board  
PFC: Perfluorinated Compounds  
PLD: Programmable Logic Device  
PWA: Printed Wiring Assembly  
PWB: Printed Wiring Board  
PTH: Plated Through Hole  
QFP: Quad Flat Package  
RF: Radio Frequency  
SA: Semi-aqueous

SEM: Scanning Electron Microscopy  
Sematech: Semiconductor Technology  
SIR: Surface Insulation Resistance  
SMD: Surface Mount Device  
SMT: Surface Mount Technology  
SNAP: Significant New Alternatives Program  
SPC: Statistical Process Control  
TAB: Tape Automated Bonding (aka TCP: Tape Carrier Packaging)  
TBGA: Tape Ball Grid Array  
TCE: Thermal Coefficient of Expansion  
TCP: Tape Carrier Packaging (aka TAB: Tape Automated Bonding)  
UUT: Unit Under Test  
UV: ultraviolet light  
VOC: Volatile Organic Compounds  
WS: Water Soluble

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