

## Evaluation of the sensitivity of newly emerging FD-SOI technologies to the combined low temperature and radiation environment in space

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### **Abstract:**

Deep sub-micron FD SOI CMOS technology is an extremely attractive candidate for future low power and high speed electronic systems for NASA missions because it offers many advantages over the partially depleted (PD) SOI or the bulk CMOS technology. Extremely small device features of the FD SOI CMOS transistors them more sensitive to low temperature effects compared to the two other technologies. At low temperatures, due to the lack of annealing of the damage, degradation mechanisms such as impact ionization, hot carrier effect and radiation induced total dose effect get enhanced in FD SOI devices resulting in the worsening of operating life and performance reliability. Reliability testing alone is not sufficient for a faster infusion of new technologies, but in addition to that, necessary technology modification must be done in order to enhance the reliability of the future FD SOI electronic systems for NASA missions in low temperature and radiation environments, as described in the Table 1. below,

Mission	Operating Temp.	Mission Temp.
Europa lander	-20 to +50 <sup>o</sup> C	-170 to -50 <sup>o</sup> C
Mars Sample Return	-40 to +50 <sup>o</sup> C	-140 to +20 <sup>o</sup> C
Pluto Flyby	-20 to +50 <sup>o</sup> C	-235 to -100 <sup>o</sup> C
Interstellar Travel	-20 to +50 <sup>o</sup> C	-250 to -150 <sup>o</sup> C

Table 1. Operating and mission temperatures for future space flight missions

SOI research at the NASA/JPL involve:

- Experimental determination of the sensitivity of deep sub-micron (0.25 μm and smaller) FD SOI CMOS technologies at low temperatures in presence of radiation. Identification of the temperature sensitive device features and parameters.
- Simulation of the FD SOI CMOS transistors with device simulator DESSIS to verify the experimental observation and results of the combined effects of low temperature and radiation as encountered by electronics in the space.
- Change/modification in device architecture, doping density/profile, shapes of the device features and device geometry on the device simulator before the actual implementation in the fabrication process.

Experiments:

State-of-the-art FD-SOI technologies are being evaluated through experimental measurements at low temperatures following exposures to radiation as encountered under space conditions. Variable temperature measurements are done on transistor test structures (fabricated at MIT Lincoln Laboratory using SIMOX wafers) in the temperature range of 79K to 300K.

Devices	Channel length	Si film	Film doping	T <sub>ox</sub>	BOX	Width
FD-SOI Transistors	0.25, 0.30, 0.35μm	50nm	3.5 x 10 <sup>17</sup> /cc	7.5nm	190nm	8μm

**Table 2. Device Parameters**

Two proton irradiation (for the TID of 150, 300, 450 and 600 kRads)are planned for December 1999 and February 2000 at the Indiana University Cyclotron in Bloomington In. Results from the

initial measurements conducted at 79, 100, 150, 200, 250, and 300K reflect the low temperature sensitivity of the device parameters such as the drain current ( $I_{ds}$ ), mobility ( $\mu_{eff}$ ), transconductance ( $G_m$ ), threshold voltage ( $V_{th}$ ), sub-threshold slope (S), and the early voltage ( $V_A$ ).

Results:

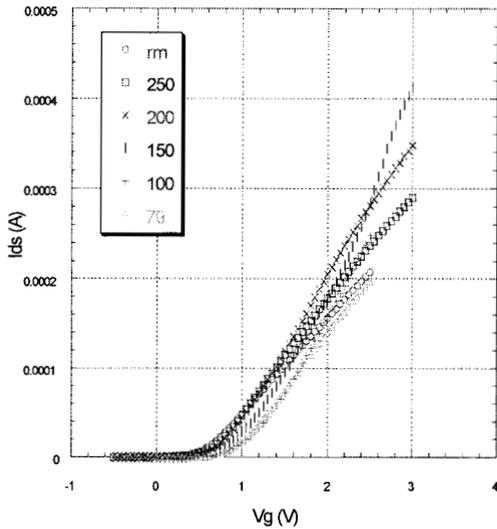


Figure 1. Drain current vs. gate voltage when the applied drain voltage is 50mV.

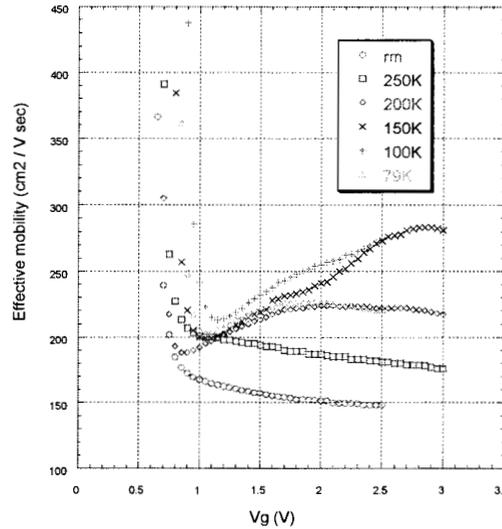


Figure 2. Effective mobility vs. gate voltage when  $V_{ds}$  is for a 0.35um transistor.

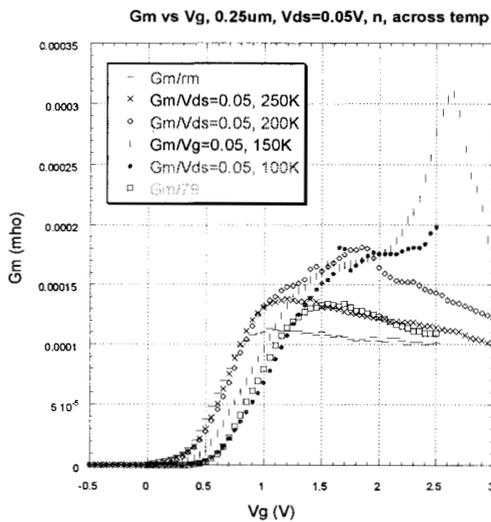


Figure 3. Transconductance vs. gate voltage for  $V_{ds} = 50mV$  for a 0.25um transistor

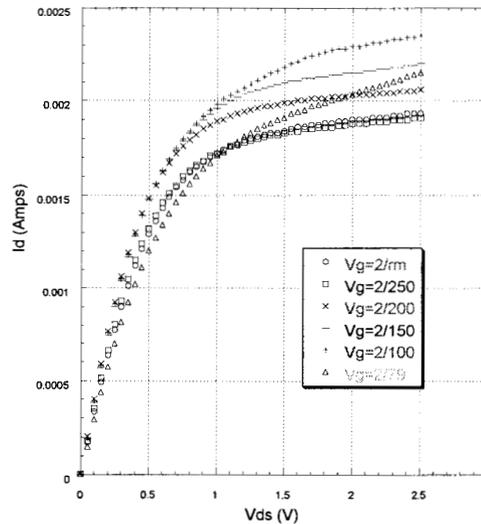
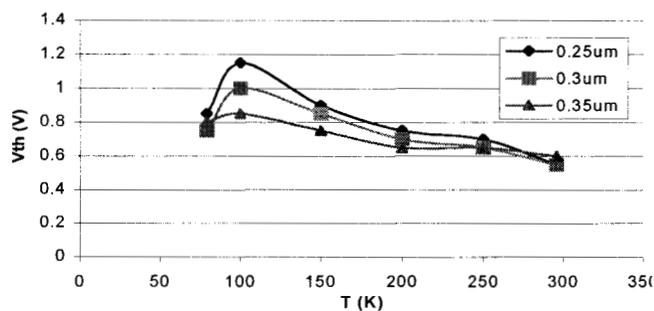


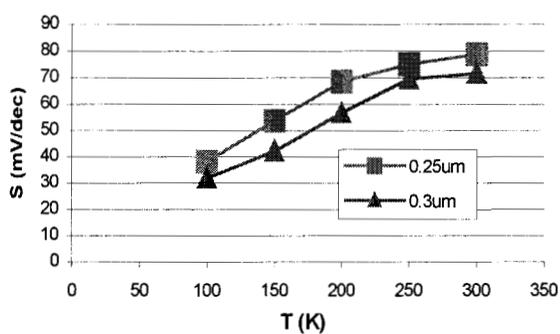
Figure 4.  $I_{ds}$ - $V_{ds}$  at  $V_g=2V$  for a 0.25um transistor

In the final paper, results from next two sets of measurements following irradiation will be presented along with the results from the theoretical simulations of devices at low temperatures with added effects of radiation. A scheme of the device modification for the radiation and low temperature tolerance will be presented in the next publication.

Following are the plots resulting from the analysis the above results. A detailed description of the analysis and the the results will be presented in the final paper.



**Figure 1. Threshold voltage vs. temperature for 0.25, 0.3, and 0.35um channel lengths**



**Figure 2. Subthreshold slope evolution vs. temperature for 0.25um and 0.30um transistors**

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