Non-Volatile Memory Slice

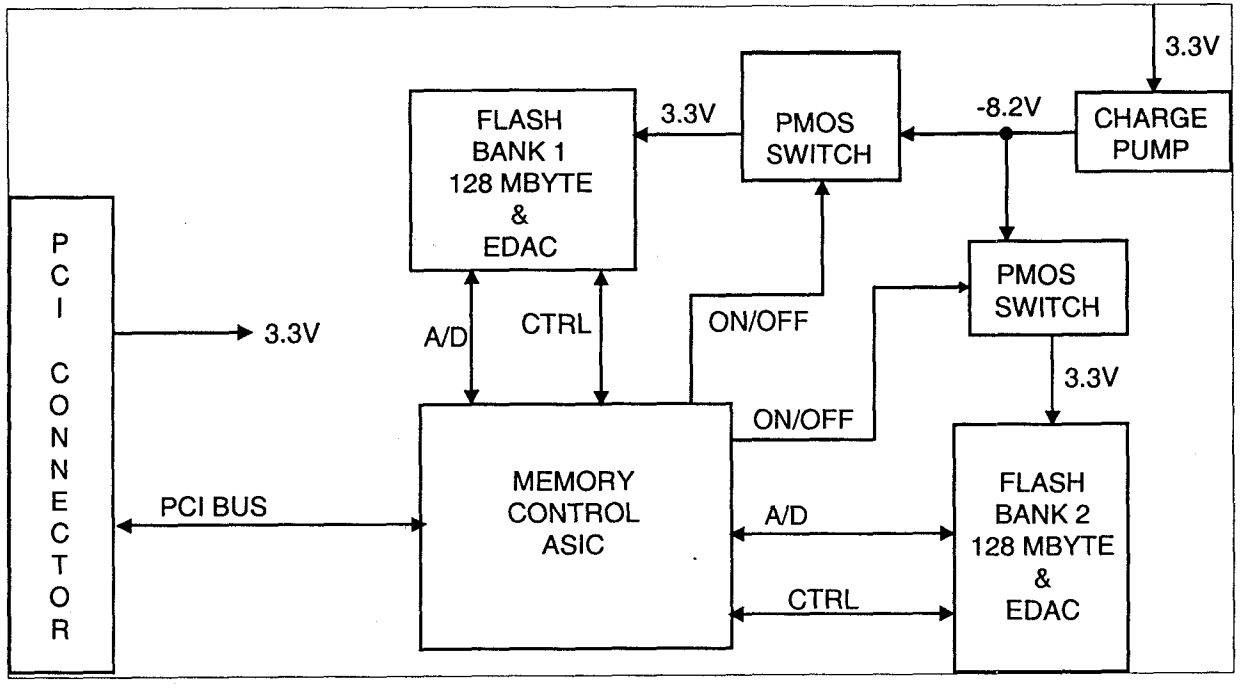
Karl Strauss
karl.f.strauss@jpl.nasa.gov

June 6, 2001

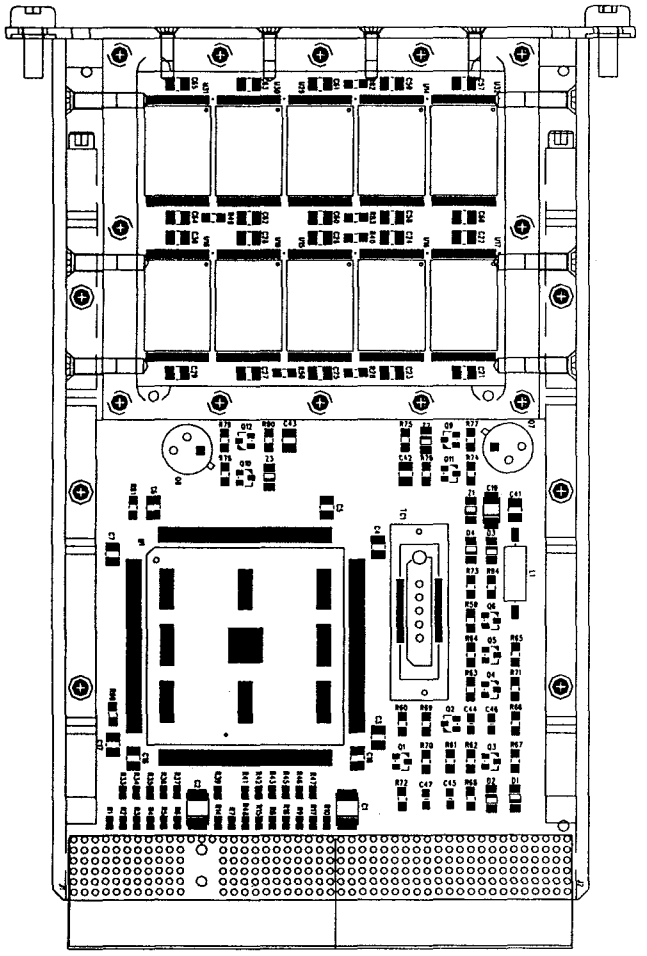
Specifications

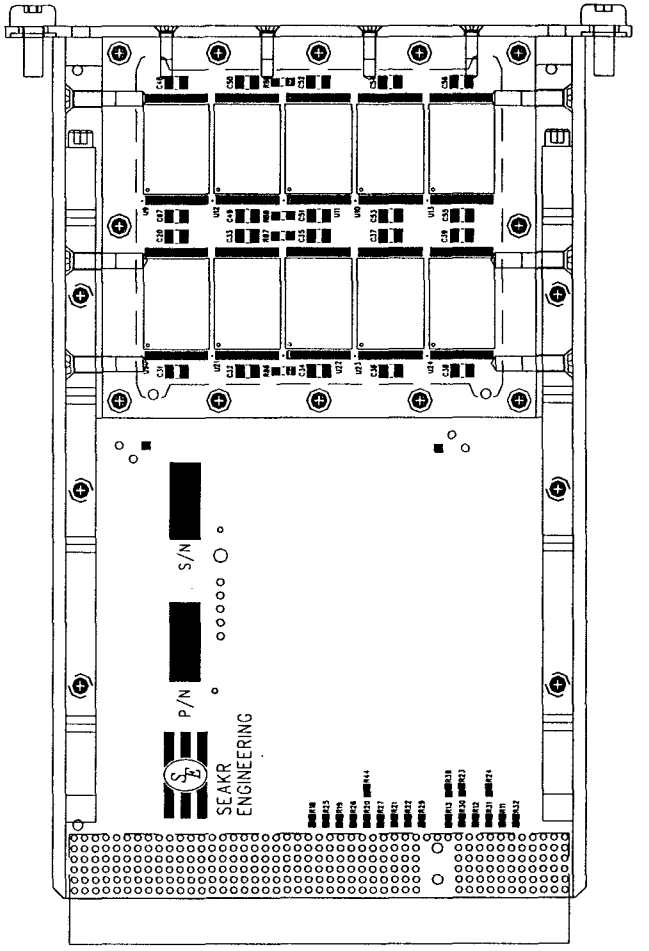
- 2 Gbit (data), Flash-based
  - Based on Samsung 128 Mbit Flash devices
  - Design can accommodate 256Mbit devices with no ASIC change
    - Equates to 4 Gbit board capacity
- Designed and Engineered by SEAKR Engineering, Englewood, Colorado
- Powerful Reed Solomon EDAC permits byte-wide loss of data with complete recovery
- Splitting of memory devices into 2 individually powered banks permits extra step of Write Protection and Power control
- At-speed PCI Interface (33 MHz)
  - Read
    - Throughput on consecutive pages 187Mbit /sec
    - 4Kbyte Burst 200Mbit/sec
  - Write
    - Throughput 27.7Mbit/sec
    - Burst 2Kbyte 1056Mbit/sec
  - Multi-bank FIFO
- Low power: 2.3 W @ 3.3 operating voltage
- 3U cPCI From Factor
  - Mass: 1661 grams with Clamshell, 340 grams without
- Radiation tolerance: 30 kRads Flash w/Clamshell, 1MRad ASIC

NVMS – Block Diagram

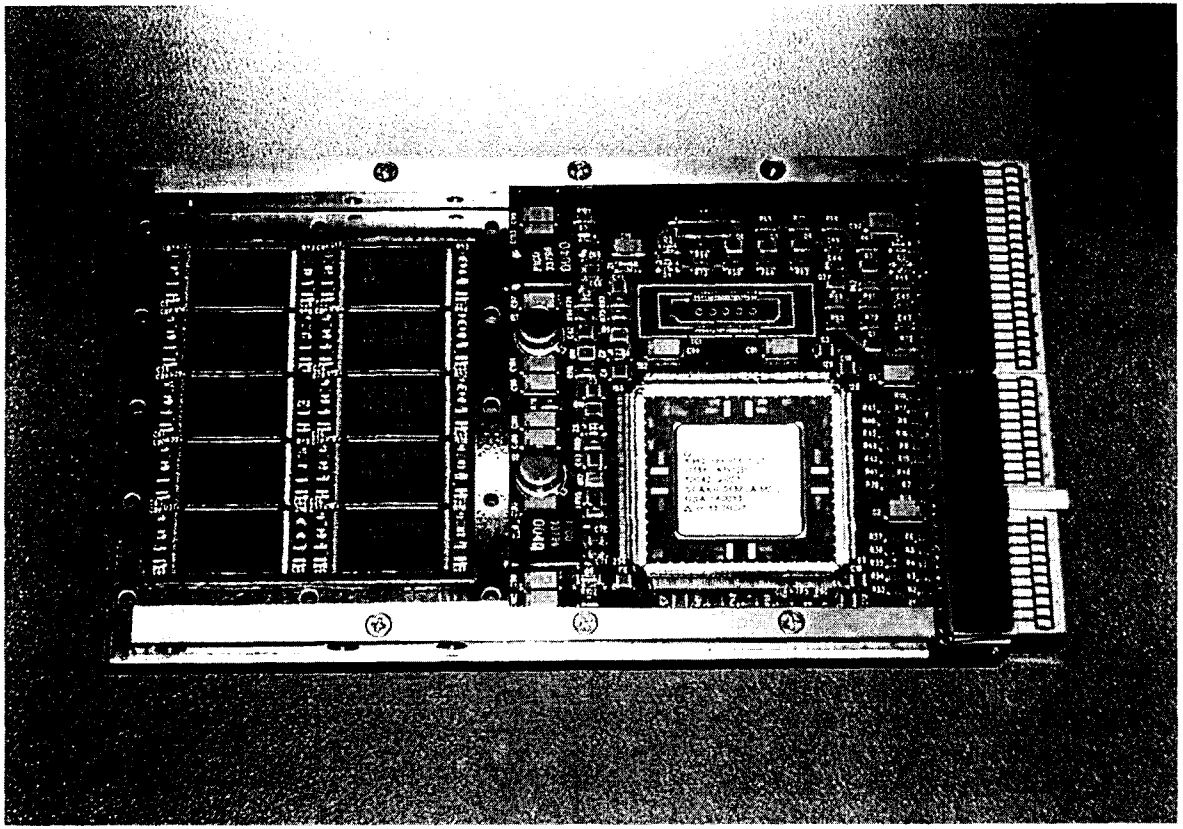


Layout

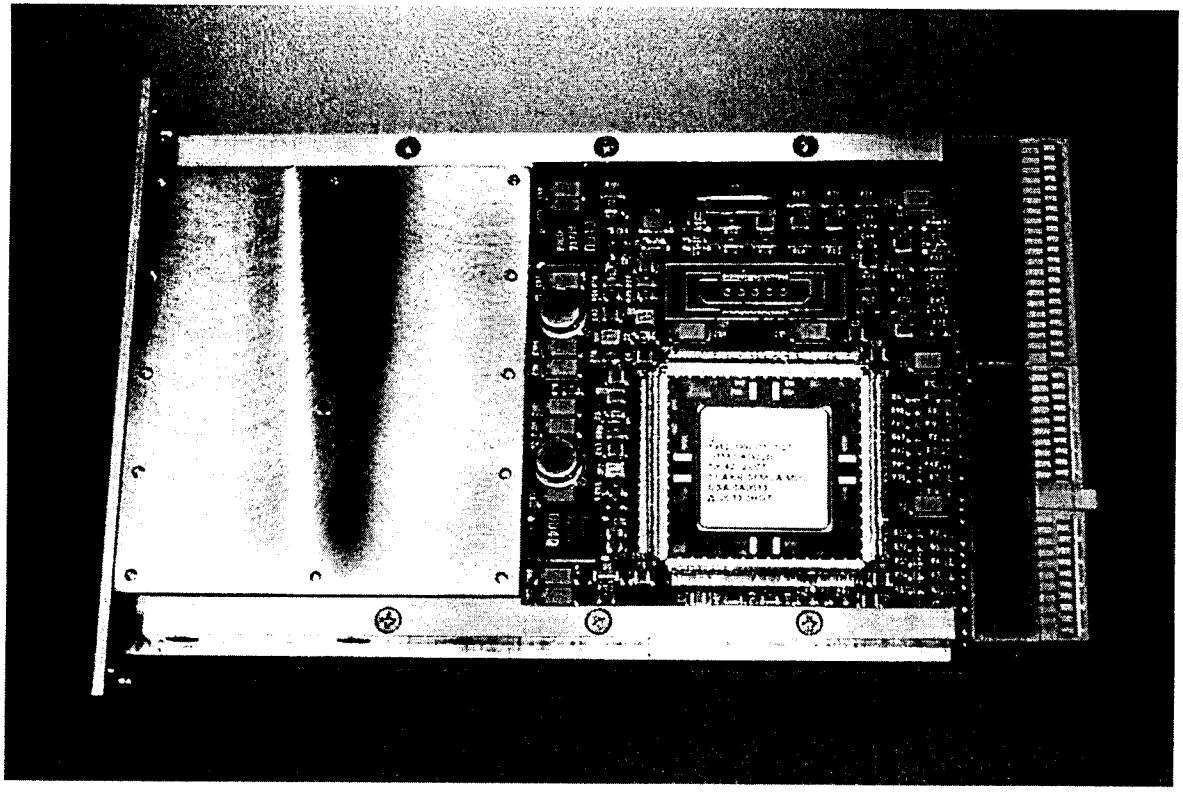




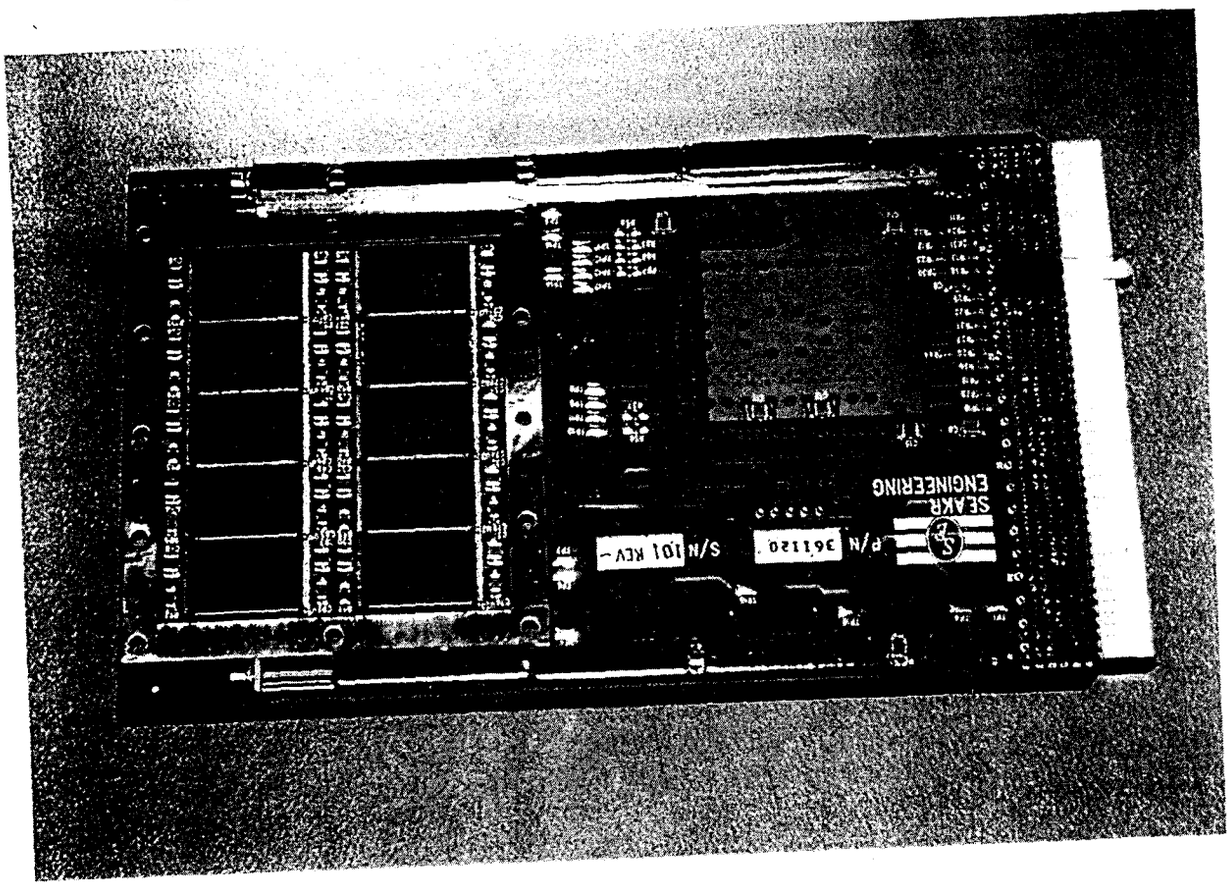
Engineering Model Board (Clamshell removed)



Engineering Model Board (w/ Clamshell)



Engineering Model Board (Reverse side Clamshell removed)



Status

- PT deliveries complete
- EM deliveries, qty 10, July 10, 2001
  - PODs in hand
  - Qual test commence end of June 2001
- FM deliveries, qty 10, November 30, 2001
  - Flight ASICs in process
    - Honeywell HX2160r
- Functional Requirements Spec:
  - JPL D-16328, rev C