SYSTEM INPUT/OUTPUT (SIO) SLICE
Description and Status

Genji Arakaki
genji.a.arakaki@jpl.nasa.gov
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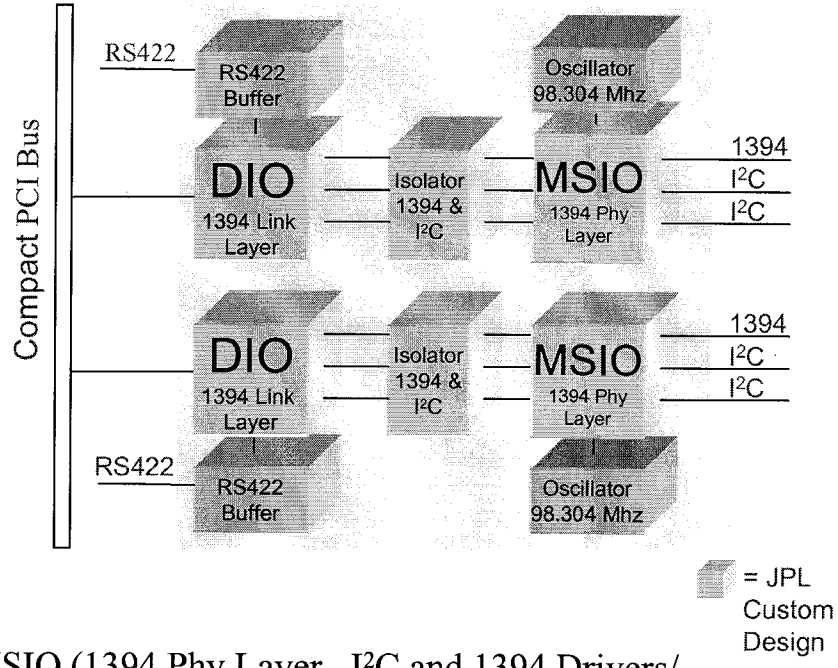
Agenda

- SIO Description
- I2C Fault Tolerance Additions
- 1394 Features
- Digital I/O (DIO) ASIC
- Mixed Signal I/O (MSIO) ASIC
- SIO Prototype Configuration
- Differences between Prototype and Engineering Model
- Engineering Model Configuration
- SIO Status
- Schedule/Milestones
- Issues and Concerns

SIO Description

- SIO Acts as the System Interface to Seven Separate X2000 Busses
  - Compact PCI bus (PICMG 2.0 R2.1)
  - IEEE 1394a Bus - 100 Mbps (2 per Slice)
  - I^2C Bus (4 per Slice)
  - Miscellaneous I/O
    - UART (4)
    - Discretes
- SIO Features
  - Double-Sided 3U Compact PCI Card
  - 1 Mrad Radiation Hardened
  - Custom ASIC, Honeywell HX3000 for DIO (1394 Link Layer , I/F to cPCI Bus, I^2C Bus Controllers, UART 16550, and Custom Logic)
  - Custom Mixed Signal ASIC, Honeywell HX2000 for MSIO (1394 Phy Layer , I^2C and 1394 Drivers/ Receivers)
  - Transformer Isolation between DIO and MSIO (1394 Link and Phy Layers, I^2C)
  - Power: 11.3 Watts Est. Max. (3.47V, Worst Case Process)
  - Mass: .5 Kg Est.
  - Ball Grid Array Packaging Technology

SIO Building Blocks



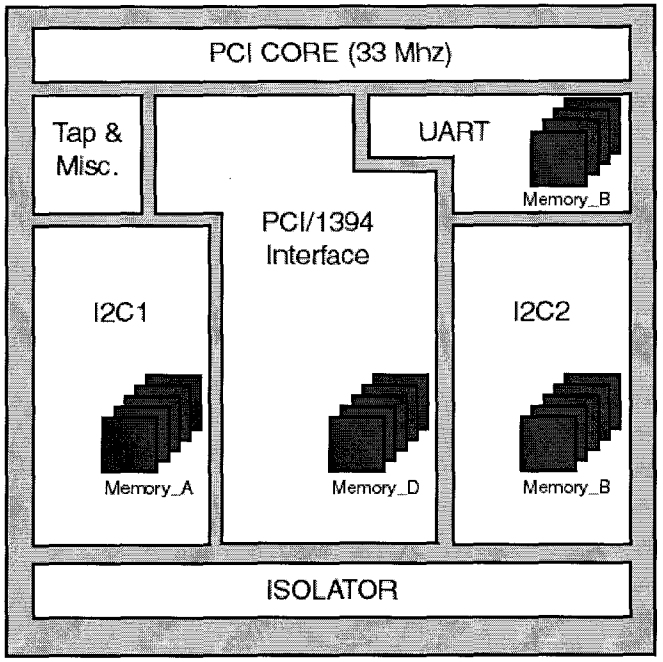
I2C Fault Tolerance Additions

- "Packetized" Data
  - Maximum Packet Size: 256 Bytes of Data
  - Byte Count and CRC Included in Packet
- "Fail Silent"
  - Hardware Implementation Requires Periodic Access to the Bus or Transmitters will be Disabled
  - If there is a "Babbler" it will Eventually Mute Itself, Allowing Bus Operations to be Resumed
  - An Implemented Set of Hardware Commands to Support This Functionality, see Full Documentation.

1394 Features

- Designed to minimize CPU intervention
- PCI bus master capability
- Sophisticated DMA logic allows large messages to be broken up / reassembled by hardware for isochronous and asynchronous operations
- DMA implementation allows selected areas of CPU / PCI address to be mapped to selected areas of 1394 address space under full control of the local CPU
  - Can map for read, write, both
- See full documentation for additional features

Digital I/O (DIO) ASIC



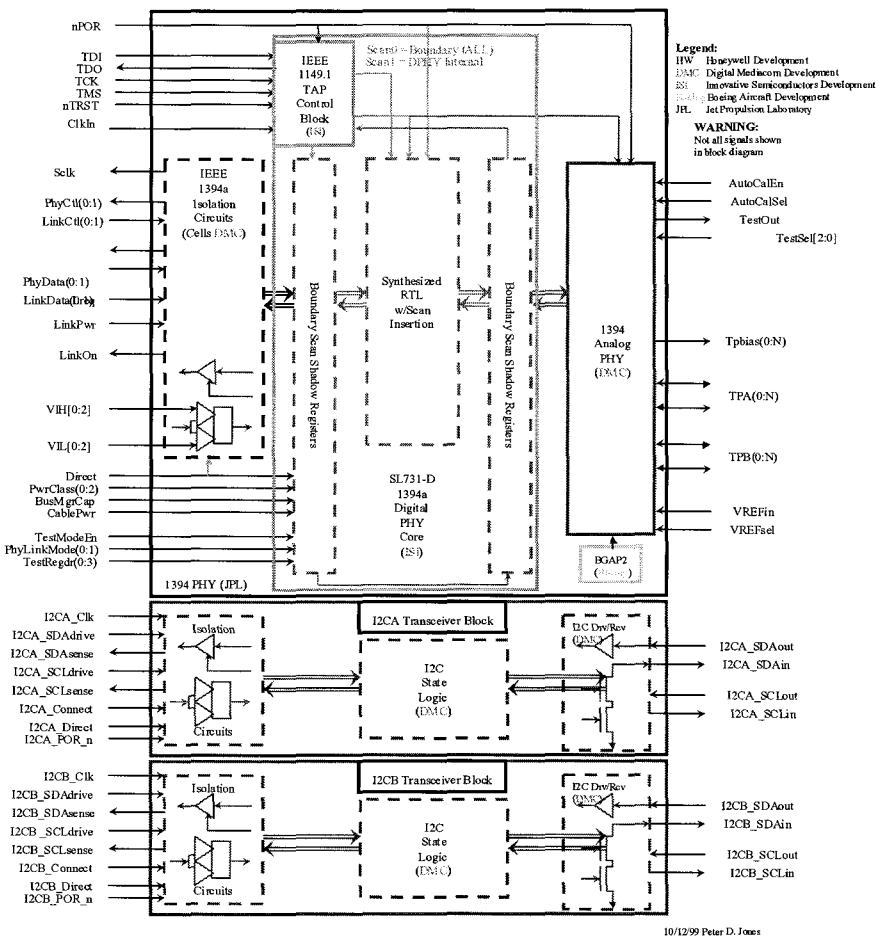
Floorplan: DIO

- Functions
  - CompactPCI Interface (33 Mhz)
  - Link & Transaction Layer of 1394 (100 Mbps)
  - I^2C Bus Controller (Hi-Rel, Fault Tolerant)
  - 16550 UART
  - Custom Logic
  - Built-in Self Test
- Design
  - JPL (Specification, I^2C High-Rel Controller, Custom Logic, Integration, Simulation and Analysis
  - Innovative Semiconductor, Inc. IP (1394 Link and Transaction)
  - Mentor Graphics (PCI, UART, I^2C IP)
- Honeywell HX3800 ASIC
  - .35 uM, SOI (Silicon-on-Insulator)
  - 1 MRrad Hardened
  - Drop-in Memory
  - Est. 700 K Gates
  - Package: 472 Pin Dimpled BGA (Ceramic)

Digital I/O (DIO) ASIC DIO ASIC (con't)

- Specifications/Documents
  - DIO ASIC Specification (JPL D-19631)
  - DIO Part Specification (JPL ST12370)
- Status
  - Pre-PDR Phase
  - Design Verification and Debug in-Process
    - cPCI, I2C, UARTs, Custom Logic Functions Verified
    - 1394 Verification Testing Nearing Completion
      - Hardware Abstraction Layer (HAL), Device Driver and Test Software Functional - 1394 Testing Accelerating
        - » Asynchronous and Isochronous Transfers during Same Cycle
        - » De-Bug and Fixes for Remaining Problems In-Process
  - Underlayers Complete

Mixed Signal I/O (MSO) ASIC



Floorplan: MSIO

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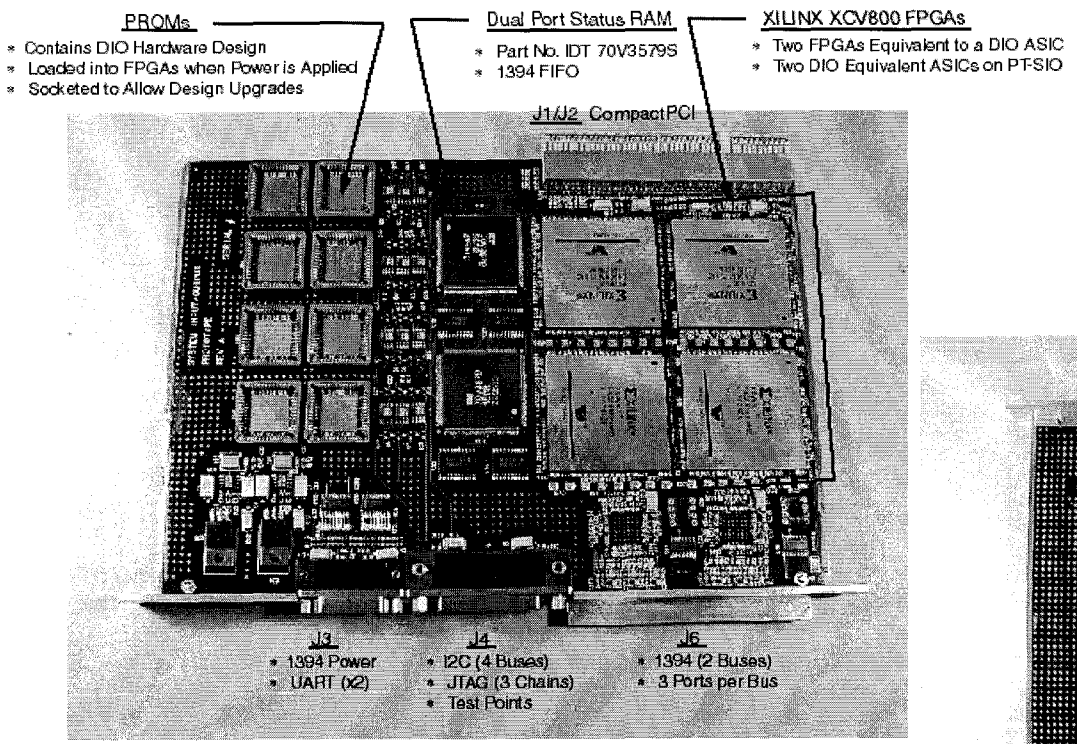
- Functions
  - 1394 S100 Physical (Phy) Layer
  - I²C Physical Interfaces
    - Slew-Rate Limited Drivers
  - Built-in Self Test
- Highlights
  - Three Separate Power Domains (1394. I²C (2))
  - I²C Fail Silent
- Design
  - Innovative Semiconductor, Inc. IP (Digital 1394 Phy Block)
  - Boeing (Voltage Reference)
  - DigitalMediaCom (Analog Physical Layer, I²C Blocks)
  - JPL In-house Specification, Integration, Simulation and Analysis
- Honeywell HX2160 ASIC
  - .7 uM SOI CMOS
  - 1 MRad Hardened
- Package: 472 Pin Dimpled BGA (Ceramic)

Mixed Signal I/O (MSO) ASIC (con't)

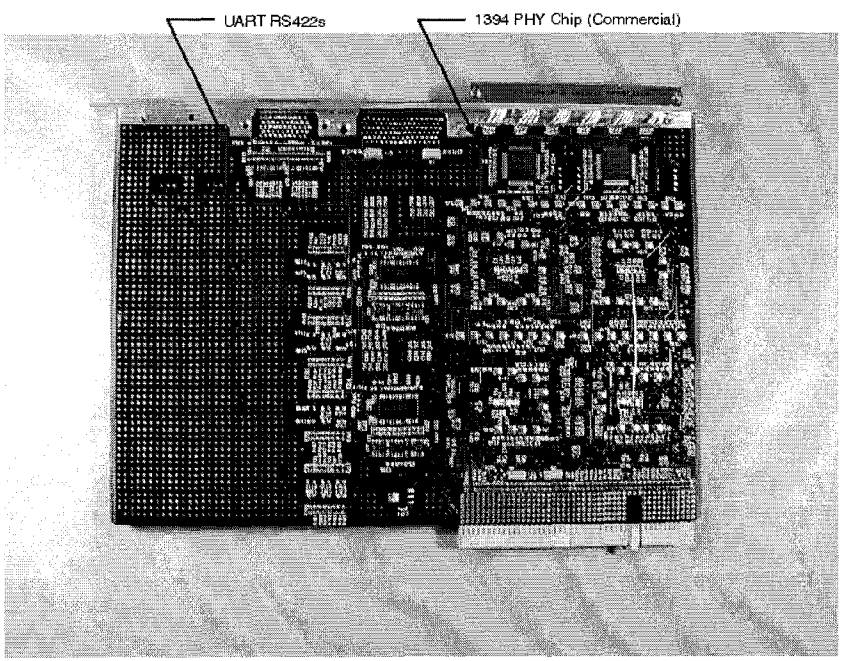
- Documents/Specifications
  - MSIO ASIC Requirements: D-18050
  - MSIO ASIC Specification: JPL D-18051
  - Procurement (ST) Specification: ST12371
- Status (June 2000)
  - Honeywell CDR Complete
    - Currently in Mask Release at Honeywell
  - Delta CDR Scheduled
    - Final Test Vectors, Test Specification

SIO Prototype Configuration



Front

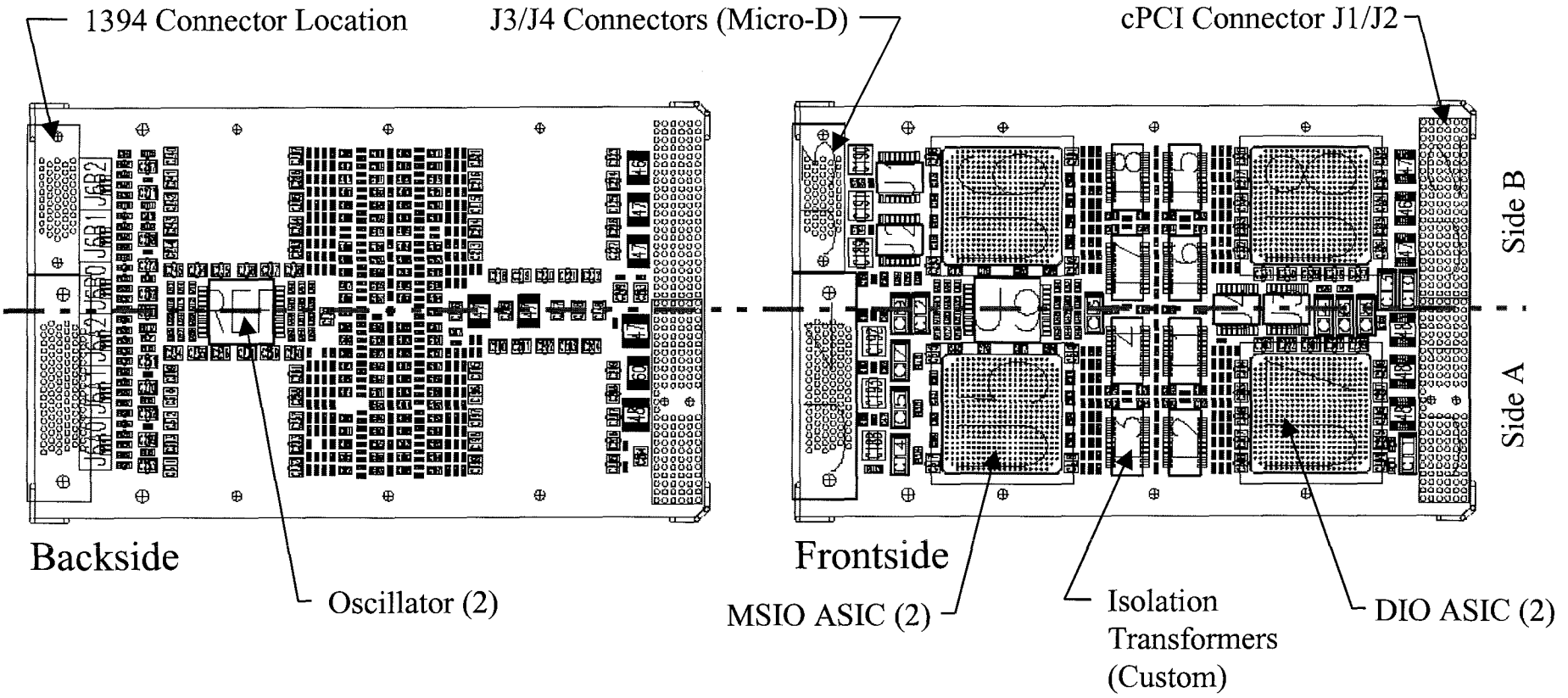
Back



Differences between Prototype and Engineering Model

Characteristic	Prototype	EM/Flight
Electrical		
- DIO	FPGA(s)	ASIC
- SRAM	External	in DIO ASIC
- Electrical Isolation	Capacitive Isolation on 1394	Transformer Isolation
	Opto-CoupleD Isolation on I^2C	
- Slew Rate Limiting	External (Discrete)	in MSIO ASIC
- cPCI Bus Speed	16 Mhz	33 Mhz
- 1394 Bus Speed	1/4 Speed (25 Mbps)	Full Speed (100 Mbps)
Mechanical		
- Form Factor	cPCI 6U	cPCI 3U
- BGA	Plastic	Dimpled Ceramic
- Electronic Parts	Commercial, Non Rad-Hard	Rad-Hard

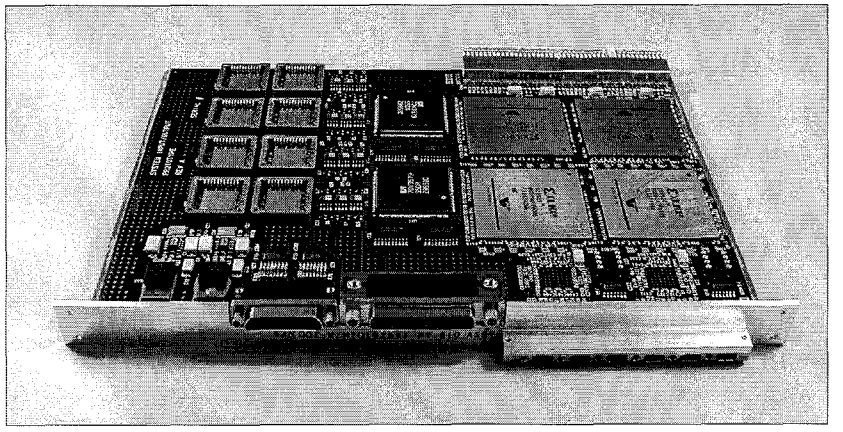
Engineering Model Configuration



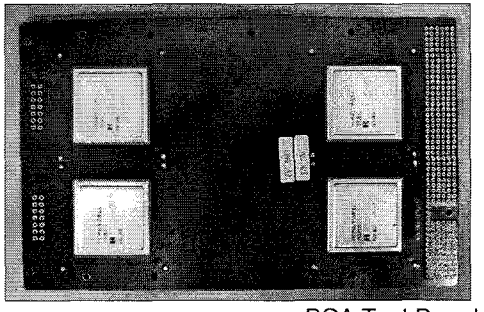
Baseline Design

SIO Status (June 2000)

- PT-SIO Serno 001-005 Delivered to Hardware Integration
  - Testing In Process
- Engineering Model/Flight Layout In-Process
- BGA Initial Process Development and Qualification Complete
  - Final Go-Ahead Pending Delta Qualification of Solder Material



PT-SIO Serno 001



BGA Test Board

Schedule/Milestones

Milestone	Date
DIO ASIC Preliminary Design Review (PDR)	7/19/01
DIO ASIC Critical Design Review (CDR)	9/12/01
SIO Slice CDR	10/11/01
MSIO POD Delivery from Honeywell	12/14/01
DIO POD Delivery from Honeywell	1/3/02
SIO EM001 Delivery to Hardware Integration	2/28/02

Issues and Concerns

- Schedule
  - Slips in MSIO and DIO Development Schedule
- Completion of 1394 Testing
  - Bug Fixes
  - Fault Cases
- New ASIC Developments
  - 1st Pass Success Required for Engineering Models
- BGA Technology
  - Minimal Flight History
- Real Estate / PWB Complexity
  - Very Tight