

RAD750 System Flight Computer

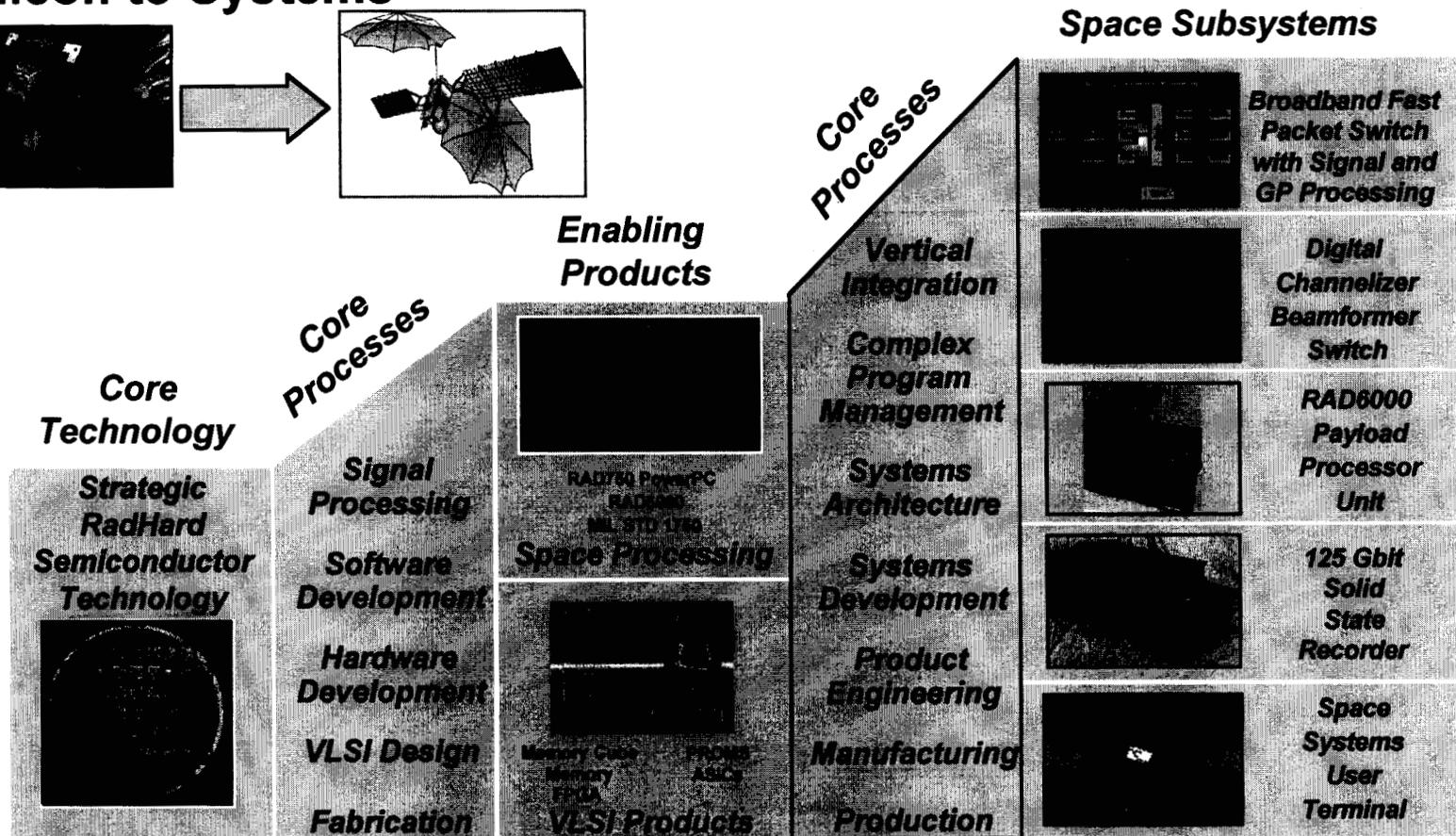
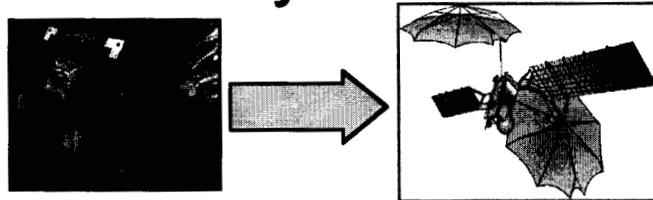
Anne Cady
BAE SYSTEMS

BAE SYSTEMS - Manassas

Capabilities

BAE SYSTEMS

"Silicon to Systems"



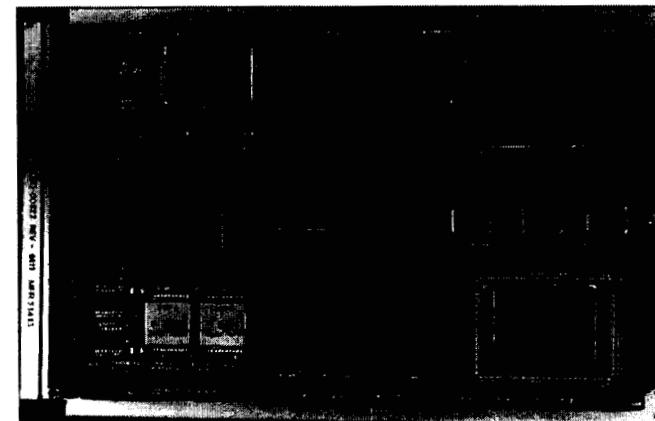
Our core processes and technologies enable a wide range of advanced systems

91 satellites currently on orbit with 287 single board computers*

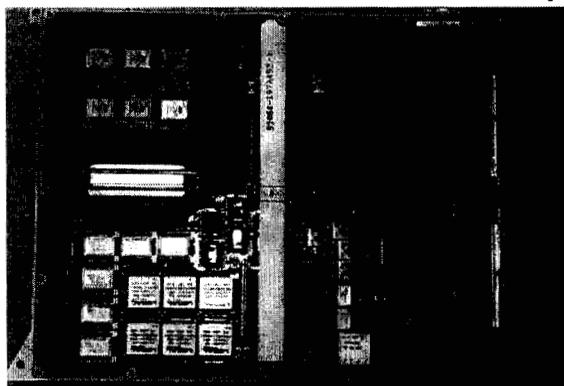
* As of January, 2002



Cassini GVSC processor

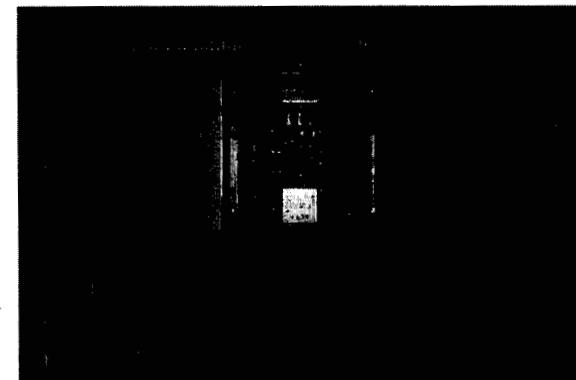


SBIRS Low/Orbview RAD6000



CCP drop in tray
(GVSC)

Over 500 flight boards delivered or ordered for new launches through 2006

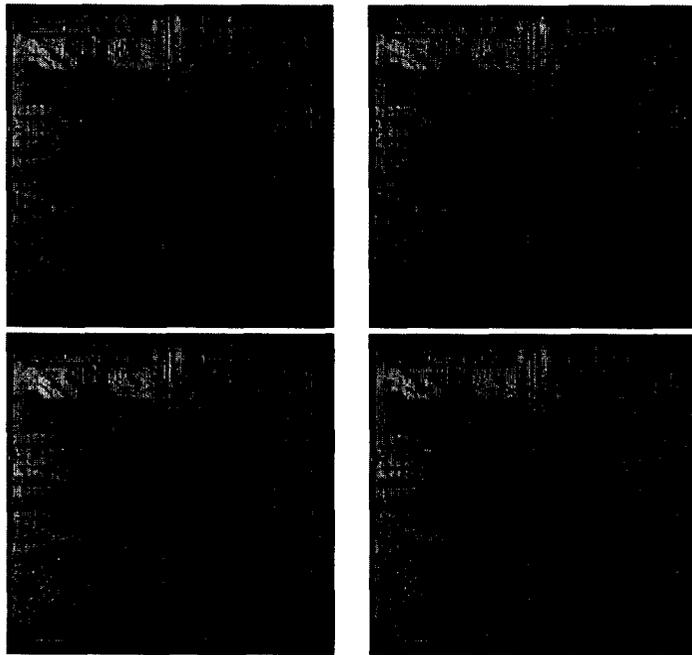


VME 6U RAD6000 board *
* as used on FHLP

Our processors have been the standard in space for many years, with millions of hours of flawless operation in a variety of applications

Three generations of radiation hardened microprocessors

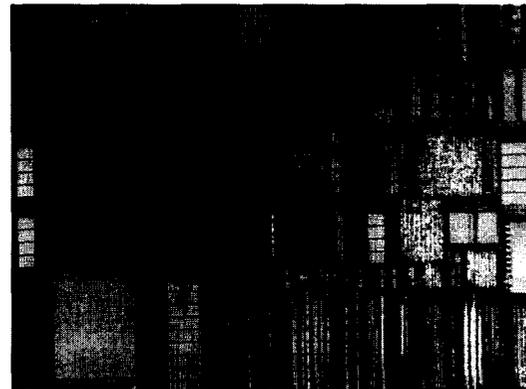
The PowerPC name, PowerPC 750, and the PowerPC logotype are trademarks of International Business Machines Corp., used under license therefrom



1991

GVSC 1750

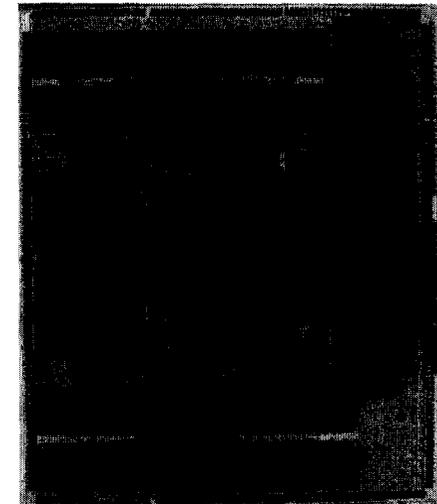
- 1.0 μ m Radiation Hardened CMOS
- MIL-STD-1750A architecture
- 4 by 88 sq mm
- 0.3 M transistors
- 20 MHz
- 3 MIPS



1996

RAD6000™

- 0.5 μ m Radiation Hardened CMOS
- RS/6000 "Power" architecture
- 145 sq mm
- 1.1 M transistors
- 33 MHz
- 35 MIPS



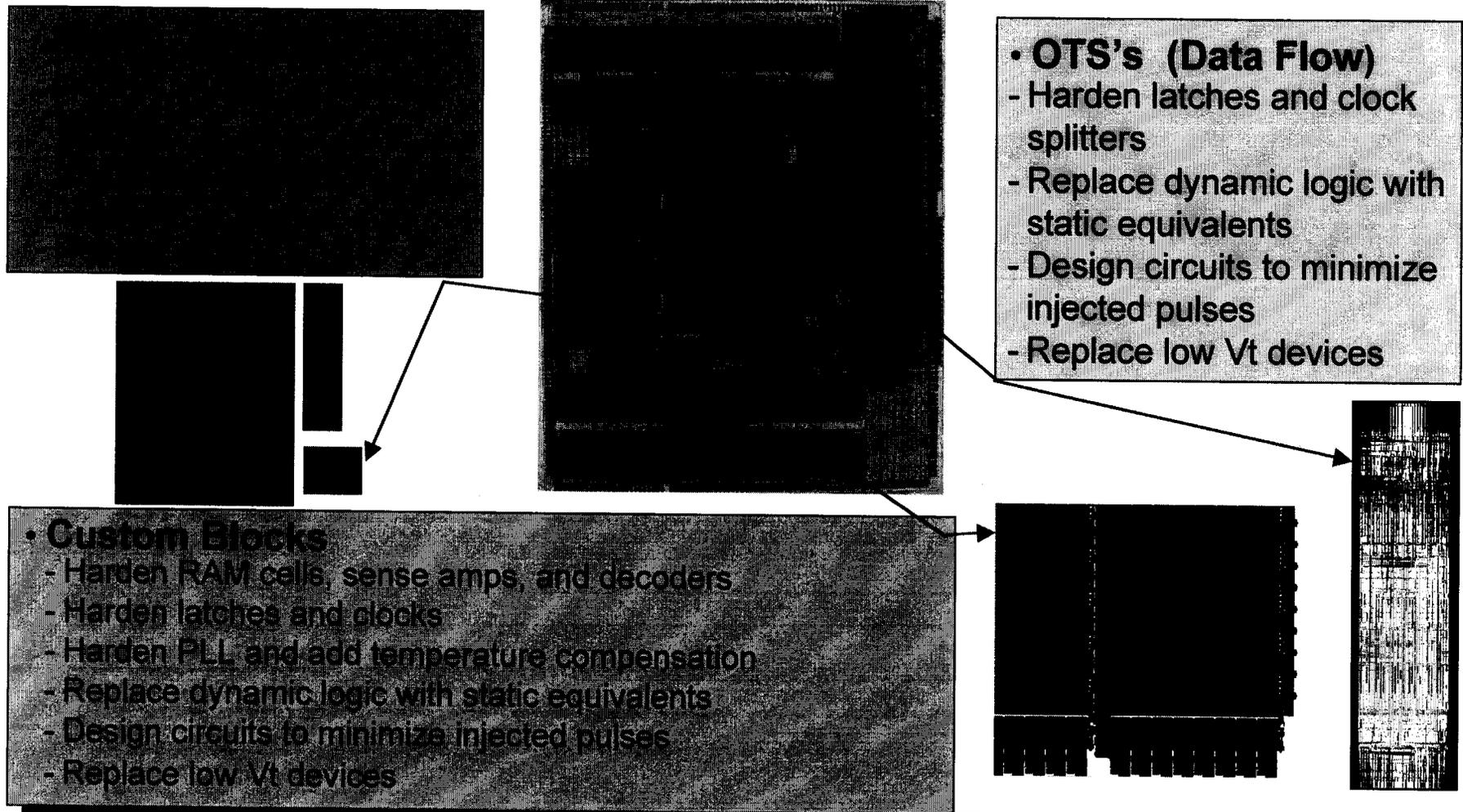
2001

RAD750™

- 0.25 μ m Radiation Hardened CMOS
- PowerPC architecture family
- 130 sq mm
- 10.4 M transistors
- 133 - 166 MHz (up to 200 as available)
- 240 - 300 MIPS (up to 366 as available)

The RAD750 represents our third generation product, with architectural and technological enhancements that improve power/performance

SEE enhancements made to the RAD750™



Customization of the PowerPC 750 to improve SEE hardness required replacement of the circuitry while maintaining identical logic function

Radiation Results for RAD750™

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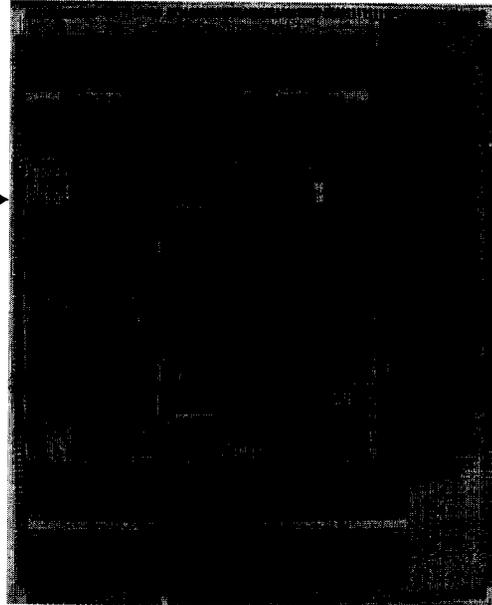
Prompt Dose

Test Specifics

- 850 pulses, widths 20-50 ns
- Dynamic FFT test at 33, 116, 133 MHz

Test Results

- >1E9rad(Si)/s at 133MHz



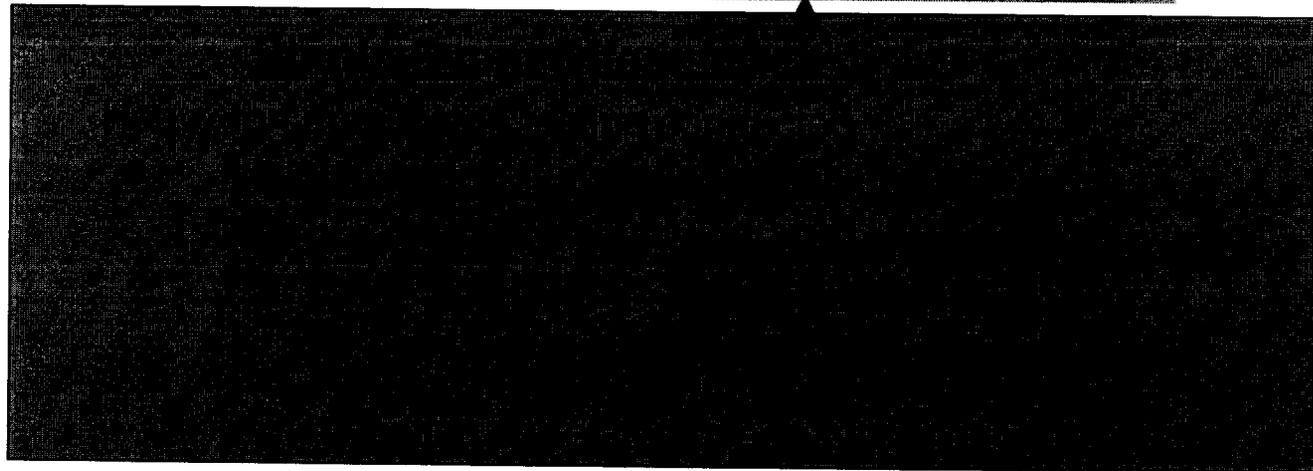
Total Ionizing Dose

Test Specifics

- 73 Rad(Si)/s and 25°C
- Static bias in Gamma Cell

Test Results:

- >200 Krad(Si)

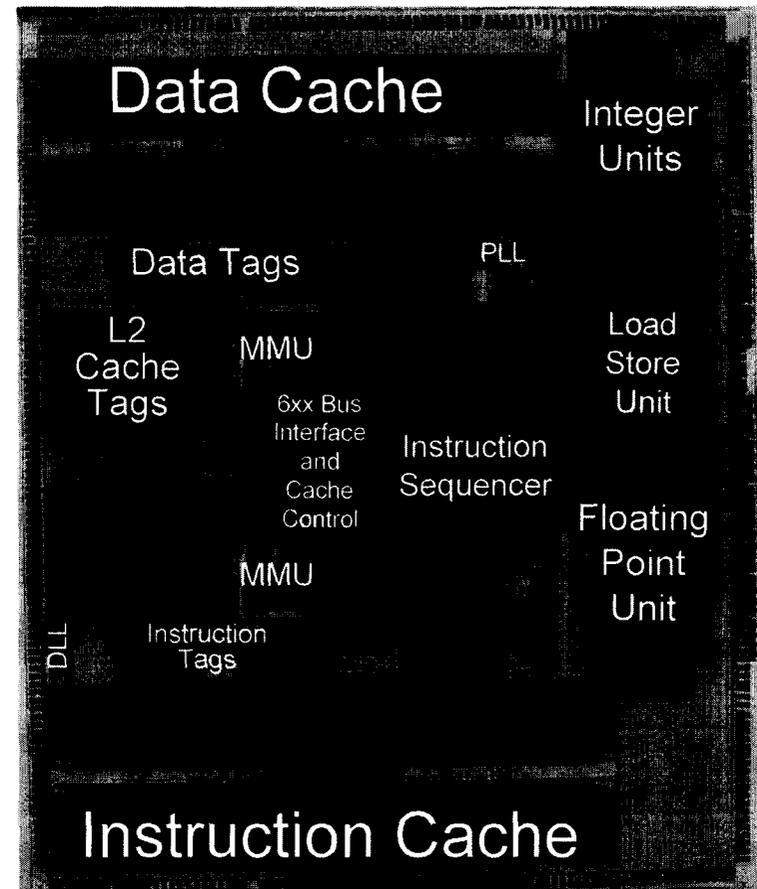


Witnessed by
General Dynamics +
NRL Independent
Consultant

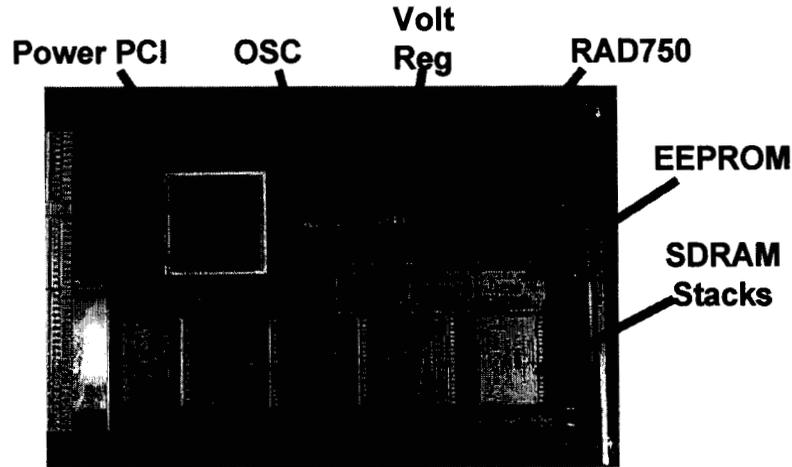
RAD750 is flight screened and available for delivery today

RAD750™ specifications

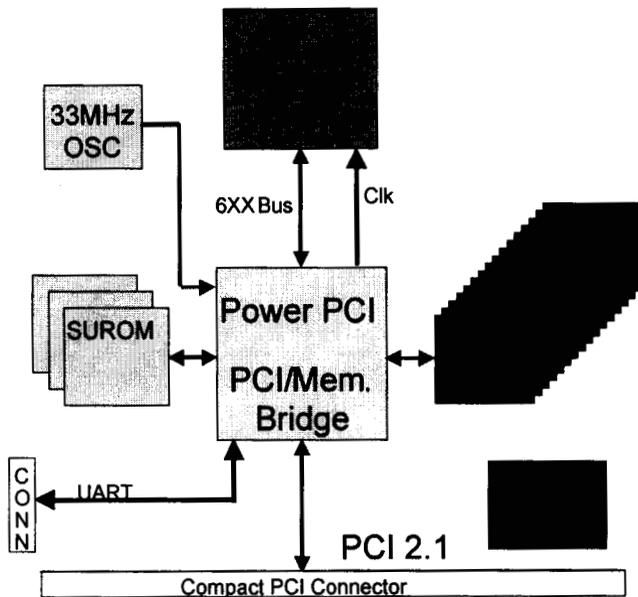
Specifications	
Processor Speed	110 to 133 MHz
Process Technology	0.25 um (0.18 um Leff) CMOS, 6 levels of metal
Die Size	10.4 mm. by 12.5 mm.
RAD750 Performance	
without L2 (est)	6.5 SPECint95 3.9 SPECfp95 @ 150 MHz.
with 1MB L2 (est)	7.0 SPECint95 4.7 SPECfp95 @ 150 MHz.
Signal I/O	256 (including L2 port)
Power Supply	2.5 V +/- 5% core 2.5 or 3.3 V +/- 10% I/O
Power Dissipation	5.0 watts at 133 MHz, 2.5V
Temperature Range	-55°C to +125°C
Packaging	25.0 mm. by 25.0 mm. by 6.22 mm. 360 pin Column Grid Array (CGA)
Mass	9.0 grams
Radiation Hardness	Total Ionizing Dose: 200 Krad (Si) SEU: 1E-10 upsets / bit-day (W.C. 90% GEO) Latchup: Immune
Mean Time Between Failures (MTBF)	> 4.3M hours



X2000 System Flight Computer Board

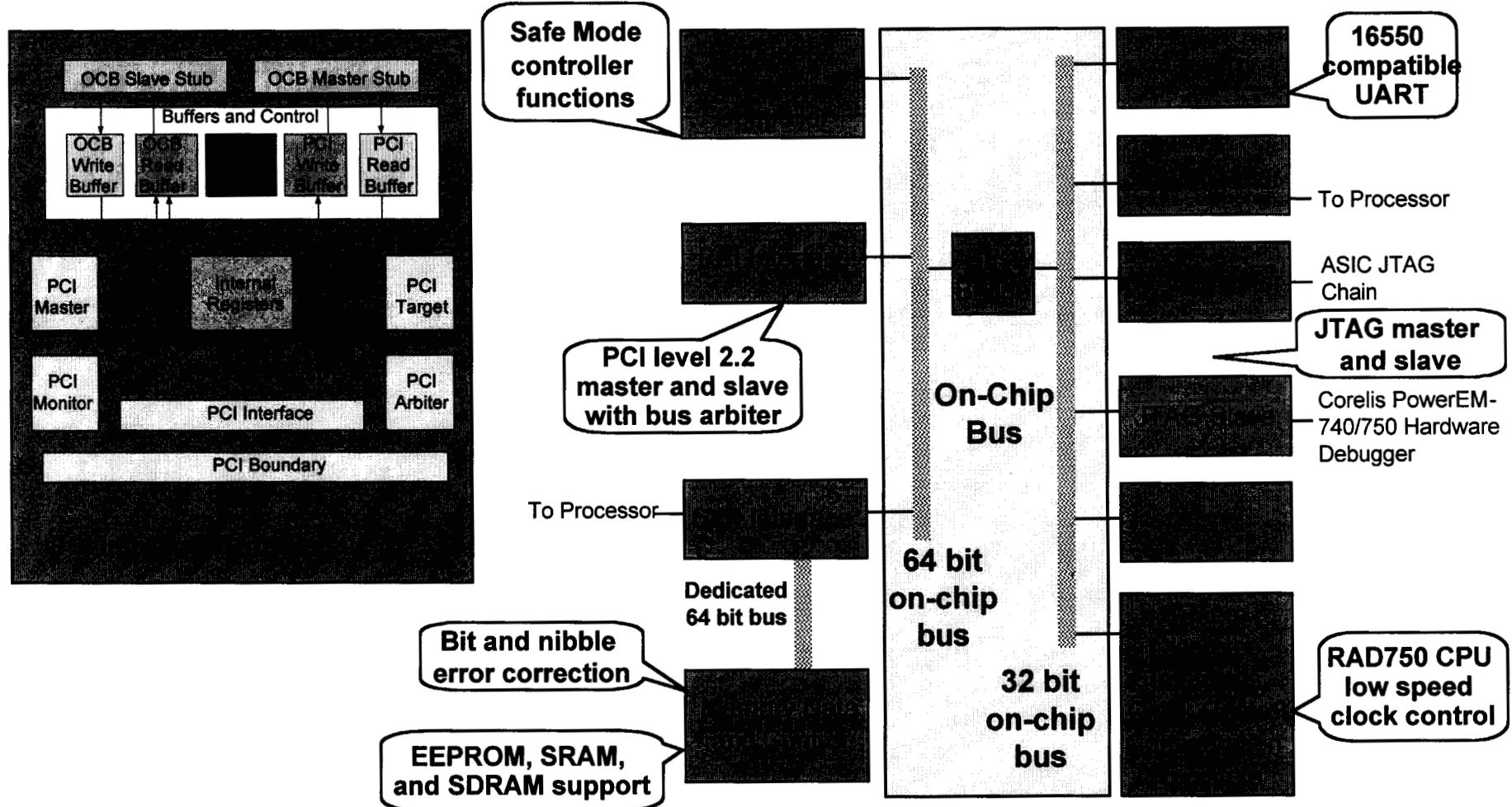


- **132 MHz RAD750 CPU**
 - 240 MIPS Dhrystone Performance
- **128MB SDRAM**
 - Uses 16Mx4 (64Mb) SDRAM packaged in 4-high stacks
- **256KB SUROM**
- **Power PCI Bridge chip**
 - Memory I/F, PCI, UART, JTAG, Timers, Programmable Interrupts/Discrettes, etc
- **Conduction Cooled, 3U CompactPCI format**
- **3.3V (+/- 10%) is only required voltage**
 - Card power <10W (*over 24 MIPS/Watt*)
- **Qual testing complete (Vibe, Pyro, Thermal Life)**
- **Over 50 cards ordered or delivered. Customers include:**
 - JPL: Europa Orbiter, Deep Impact, ST3, and Mars
 - BAE SYSTEMS - Johnson City: Bold Strike Force
 - Also Lockheed Martin, Spectrum Astro, NRL, LaRC, Raytheon, ITT and others



Flight Unit Configuration

Power PCI functional block diagram

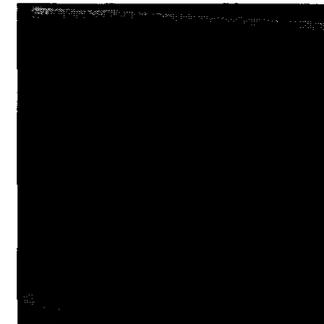
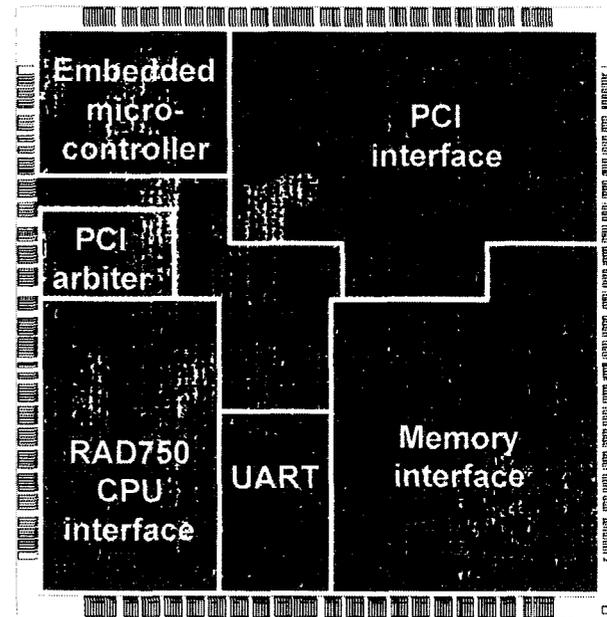


The reusable logic core architecture in the Power PCI provides for future enhancements as well as future product variations

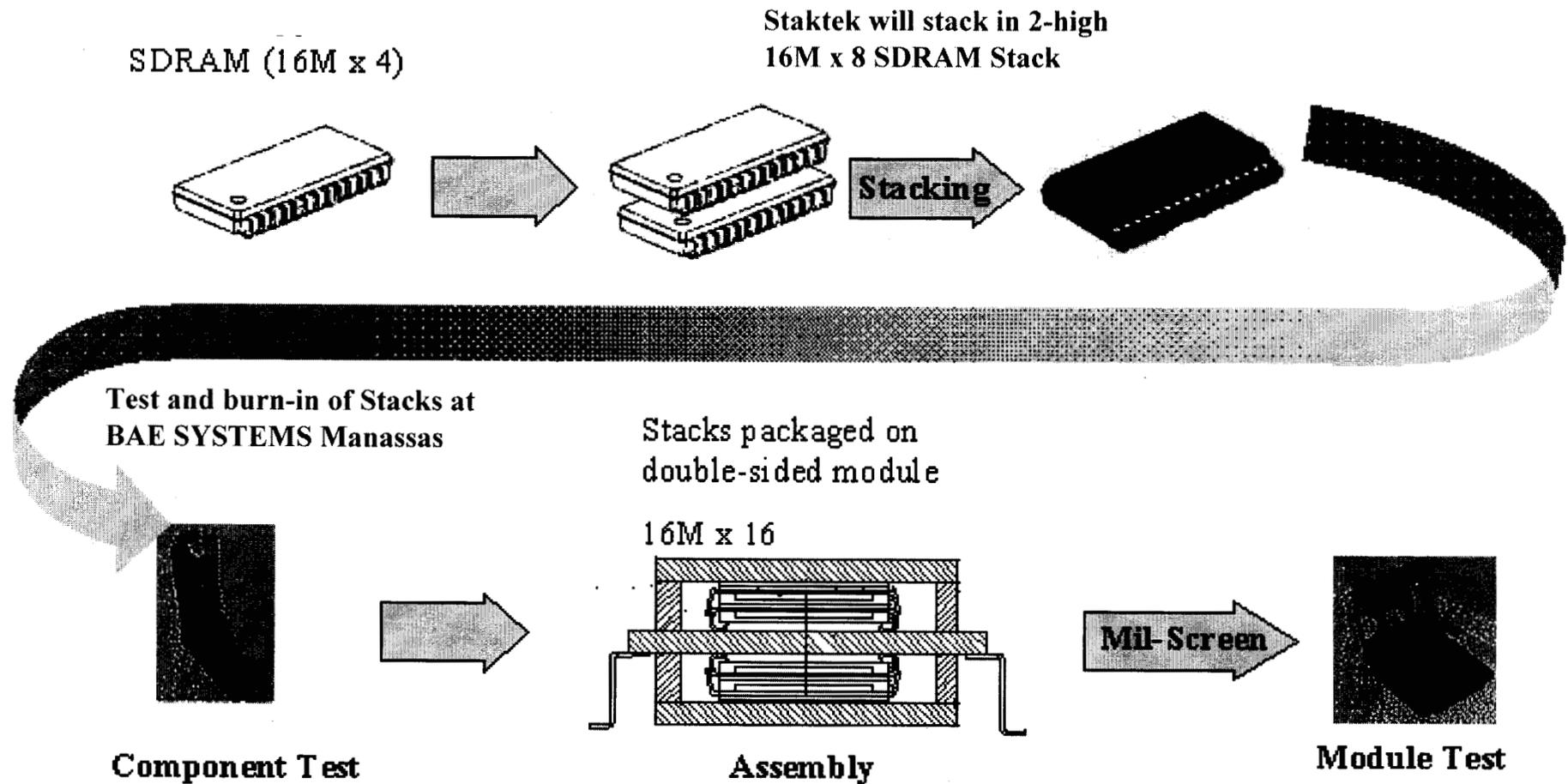
Power PCI ASIC specifications

Specifications

Clock Speed	33 MHz
Process Technology	0.50 um Leff CMOS, 5 levels of metal
Die Size	12.7 mm. by 12.7 mm.
Cells / Gates / Latches	926K / 700K / 26K
PCI Peak Bandwidth	130 MB/s write 90 MB/s read
Signal I/O	456 (+ test)
Power Supply	3.3 V + / - 10% core and I/O
Power Dissipation	1.5 W
Temperature Range	-55°C to +125°C
Packaging	32.5 mm. By 32.5 mm. By 6.22 mm. 624 pin Column Grid Array (CGA) with flip-chip C4 mount
Radiation Hardness	Total Ionizing Dose: >1Mrad (Si) SEU: < 1E-10 upsets / bit-day (W.C. 90% GEO) Latchup: Immune
Mass	14.5 grams



SDRAM Packaging



Design Status

- **Power PCI design, fabrication and testing completed**
 - Initial Power PCI Design completed and delivered to customers 1Q2001
 - 2nd version (minor backend changes) completed and delivered to customers on boards 4Q2001
 - Flight part screening complete and parts in stock
- **Board design completed and tested**
 - First SFC (Engineering Model) delivered to JPL in December 2000
 - Qualification Testing completed in September 2001
 - Six SFC Engineering units retrofitted with 2nd version Power PCI delivered to JPL in December 2001-January 2002
- **Flight Model deliveries scheduled for Late March/Early April 2002**
- **Work underway on Enhanced SFC**
 - 66MHz Enhanced Power PCI ASIC release to manufacturing expected in June 2002 (6 months ahead of schedule)
 - Enhanced SFC deliveries planned for December 2002-January 2003 (6 months ahead of schedule)

RAD750™ development software and RAD6000™ migration

Existing RAD6000

software

- VxWorks Operating System
 - Simulator
 - Interactive command shell
 - Download tools
- Green Hills Compiler Suite
 - C/C++ and Ada support
 - Compiler, linker, assembler and GUI debugger
- Board Support Package
 - MIL-STD-1553 device driver
 - IEEE-1394 driver
 - ASCM module bus driver
 - RS-232 driver
 - High Speed Serial driver
 - RAMIX Ethernet Support
 - SUROM code
- Documentation
 - RAD6000 user's guide
 - Device driver user's guides
 - Training sessions available

Existing RAD750 software

- Embedded Operating Systems already ported to the PowerPC 750 processor
 - VxWorks, LynxOS, Linux, OS-9, Chorus
 - Customers free to choose
- Compilers already ported to PowerPC 750
 - Green Hills, GNU, IBM, Diab, Cygnus, Metaware, SDS
 - Full optimization compatibility
 - Customers free to choose

–RAD750 software plan

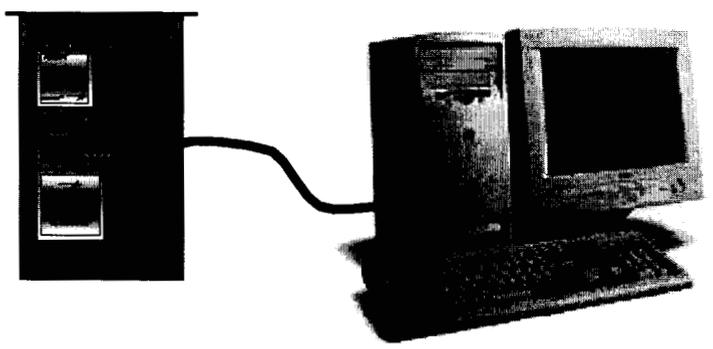
- Work with vendors to ensure full product support
- Provide Power PCI API with a superset of RAD6000 LIO capabilities
- Update Board Support Package (BSP), Start Up ROM code and RS-232 driver
- Update additional device drivers as requested by users

Ease of software port to RAD750

- RAD6000 instruction set is almost identical to RAD750
 - High level language application code ports easily
 - Assembler code ports directly, with only minor changes
 - Compilers support both ISA's with command line options

Many RAD750 operating systems and compilers are available, and software already written for the RAD6000 is easily migrated to the RAD750

RAD750™ software development environment



Software Development System

- Pentium personal computer
- Windows NT Operating System
- Ethernet connection to RAD750
- Corellis JTAG interface
- RAD750 or COTS PowerPC Board

Green Hill Multi and GNU Tools

- Optimized C, C++, Ada compilers
- Source level debugger
- Mixed language integration
- Version control system
- Program builder
- Editor

WindRiver VxWorks OS

- High performance multi-tasking kernel
- Networking capability
- Device independent I/O
- Dynamic load of user programs
- Highly configurable execution environment
- "Tornado" Software development and debug tools

BAE SYSTEMS Supplied Software

Board Support Package (BSP)

- VxWorks compatible

I/O device drivers

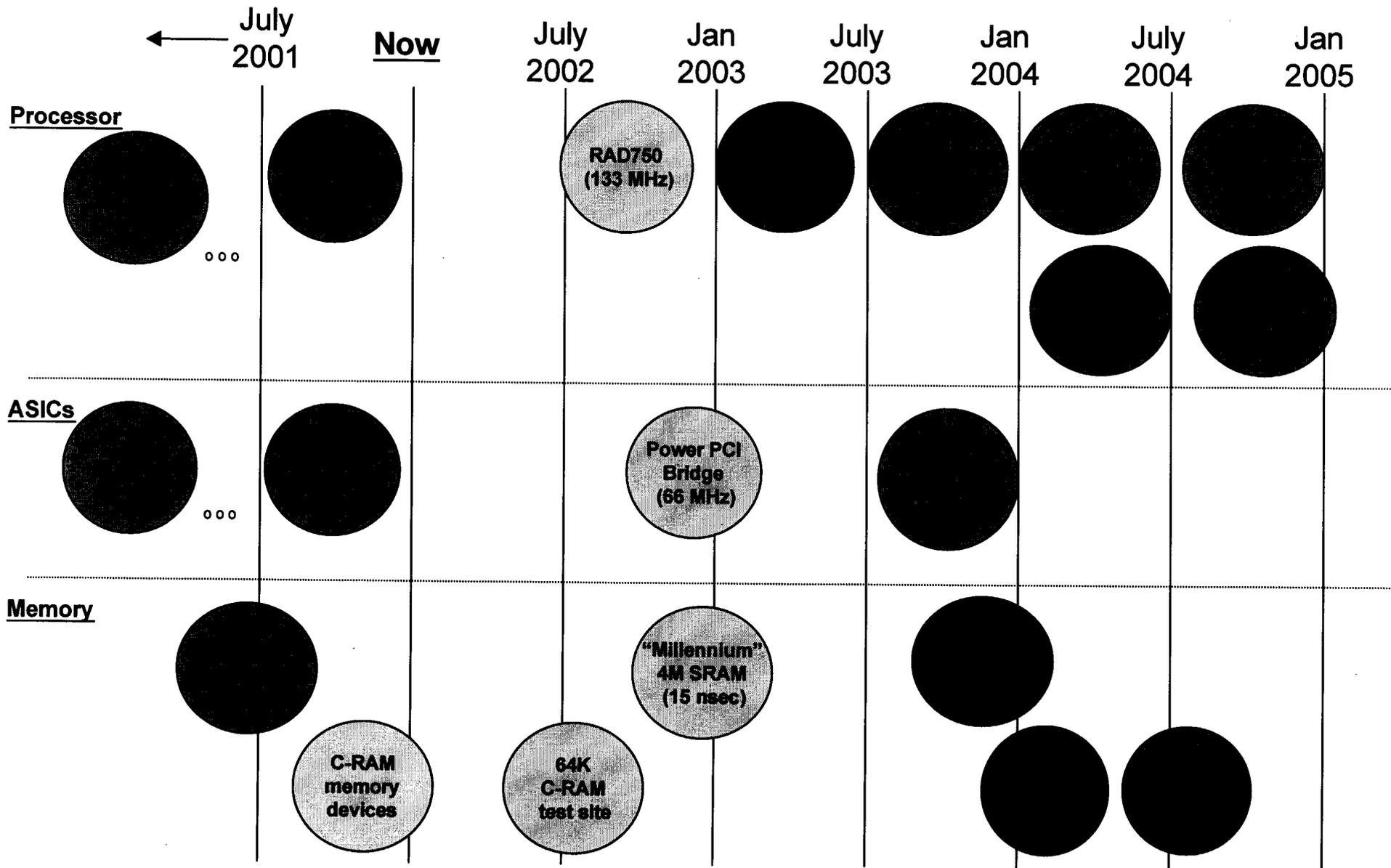
Start-Up ROM (SUROM)

- System "Reset handler"
- On-board diagnostics
 - CPU and Power PCI self-test
 - Memory test
- Bootstrap image load into RAM
- Test and initialize board hardware
- Fault recovery during restart

A complete environment, based on our RAD6000 experience, eases RAD750 software development

Processor Roadmap 2001-2005

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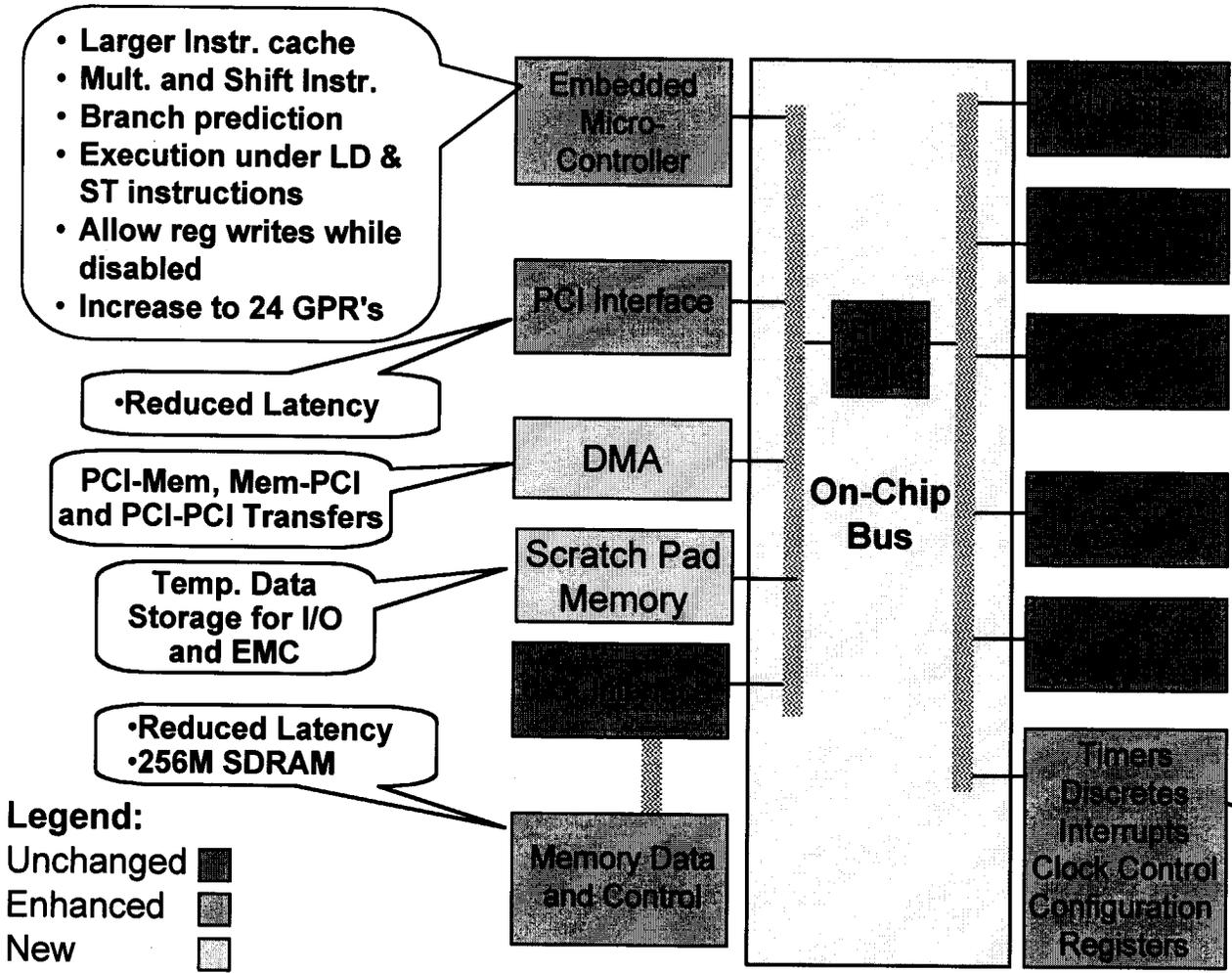


Enhanced Power PCI - Under Development

Enhanced Bridge

- Development underway under JPL funding
- Migration to R-25
 - 3.3V I/O Operation
 - 2.5V Core
- 66 MHz I/F Operation
 - Oscillator
 - 6xx Bus
 - Memory bus
- Errata Fixes
- Performance Enhancements
- Pin Compatible with Current Design

- New Interrupt Mapping
- Open Drain PIDS
- Off-card SUROM

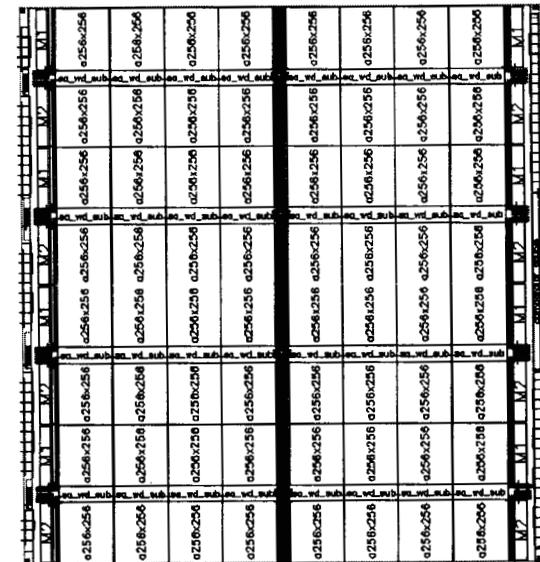
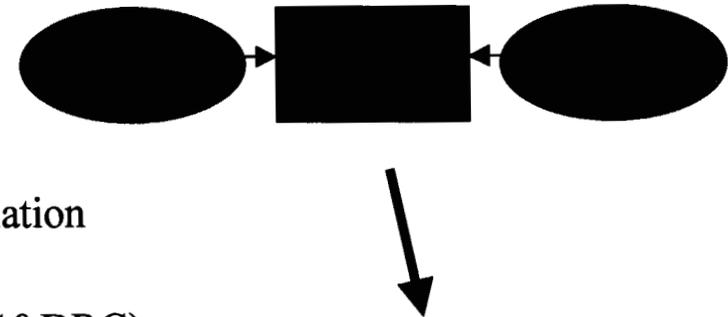


Legend:
 Unchanged
 Enhanced
 New

The Power PCI / 66 adds on-board DMA and scratchpad memory in addition to improved performance in many existing functions

L2 Cache Design Approach

- Proof of Concept
 - Use L2 Tag as Baseline SRAM Core
 - Simulate L2 Cache HLM with 750 HLM
 - Translate into Logic and Optimize
 - Architectural Tradeoffs, Circuit Design and Simulation
 - Chip Layout
 - Parasitic Extraction and Design Verification (LVS&DRC)
 - Postprocessing, Masks, and Fab
 - Initial Electrical Test
- Characterization & Radiation Testing
 - Electrical Characterization
 - SEU Test
 - Total Dose Test
- Release to Production
 - Production Design Enhancements
 - Production Test Program
 - 24 Month Overall Schedule



RAD750 L2 Cache CGA MCM

- **42.5 mm CGA Module Contains:**
 - 1 RAD750
 - 2 L2 Cache Memory (1MB total)
 - RAD750 package capacitors
- **CGA Design Features**
 - Pin for Pin with existing RAD750 package
 - Proven Design and Process
 - Builds on current X2000 CGA family
 - 25mm CGA used for RAD750
 - 32mm CGA used for Power PCI
- **Task Elements**
 - Development & Implementation (Leverage L2 Tag design)
 - Test and Screen
 - Qualification & Board Evaluation



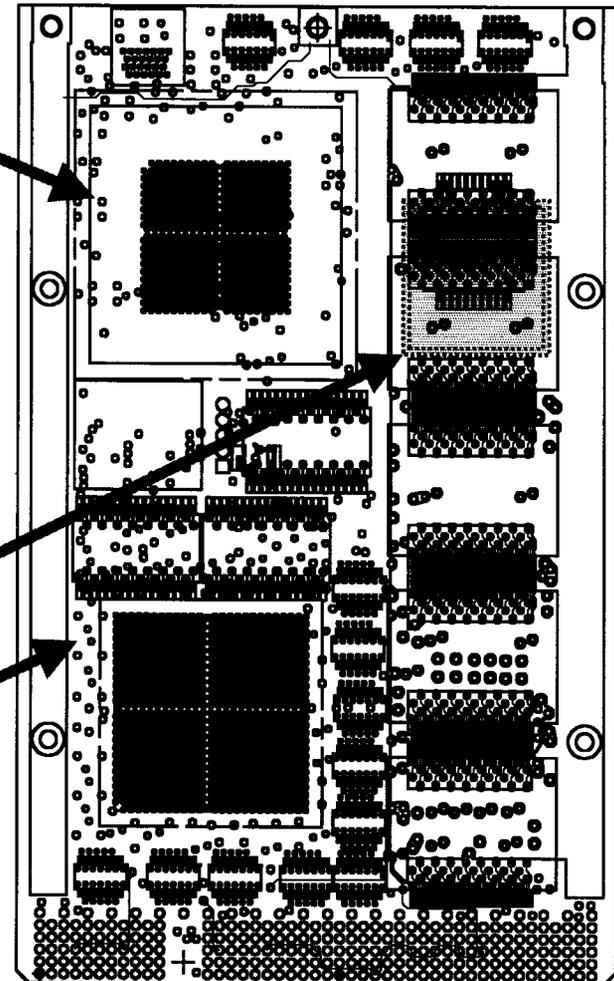
42.5 mm CGA

RAD750 / L2 Cache MCM

Leveraging the dedicated L2 cache port on the RAD750 with radiation hardened memory chips will further extend the processor's performance

RAD750 with L2 Cache 3U Board

- Multi-chip package approach with the RAD750 and two L2 cache chips placed in a 42mm ceramic column grid array package.
- Printed wiring board stack-up, wire size and spacing rules will be the same as those used on X2000 SFC design.
- No buried or blind vias.
- Oscillator moved to back side of board
- EEPROM parts rearranged on board



The MCM will fit on a CompactPCI 3U board, allowing “drop-in” upgrades

Memory options becoming limited

	Speed	Power	Cost	Cycle Life	Non-Volatile
SRAM	Very High	High	High	Very High	No
DRAM	High	High	Very Low	Very High	No
FLASH	Low	Very Low	Low	Low	Yes
OUM	High	Low	Very Low	High	Yes

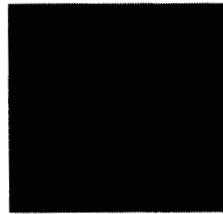
- DRAM (SDRAM) - Volatile, significant power, Low radiation tolerance-susceptible to stuck bits
- SRAM - Lower density, high power, Volatile
- Flash - Limited cycle life, low speed
- ***Ovonic Unified Memory (Chalcogenide) offers a solution - high speed, low power, high cycle life, non-volatile and radiation hardened to substrate limit***

Chalcogenide-Based Non-Volatile Memory Technology

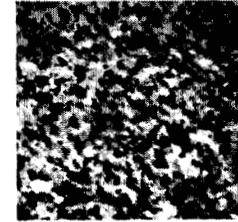
- **Chalcogenides:**

- alloys with at least one Group VI element that can exist in either of two stable state

Amorphous State
Low reflectance & conductance



Polycrystalline State
High reflectance & conductance

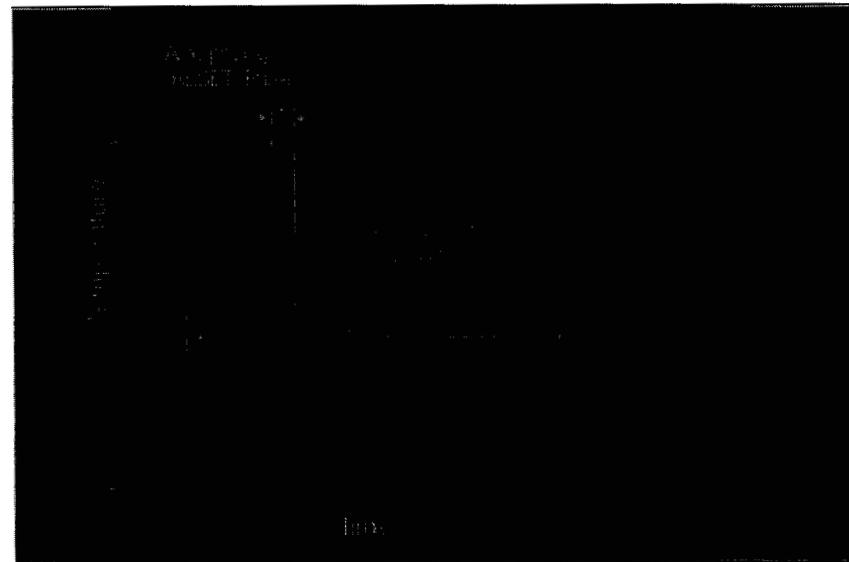


- **To change states:**

- to set (amorphize), melt alloy and remove heat
- to reset (crystallize), raise to a lower temperature and then remove heat

- **to Read:**

- apply low voltage. Electric current determined by resistance of memory element



Current Status

- **Phase 0A Complete**

- Memory cell demonstrated with good uniformity, endurance, write/read power

- **Phase 0B Started**

- Design and fabricate test chips which:
 - Integrate memory cell with CMOS transistors
 - Target device sizes support 16Mb arrays in 0.5 micron CMOS
 - Demonstrate write & read peripheral circuitry
- Test chips focused on integrating all elements by end of Phase 0B (64kb arrays)

- **Recent Progress**

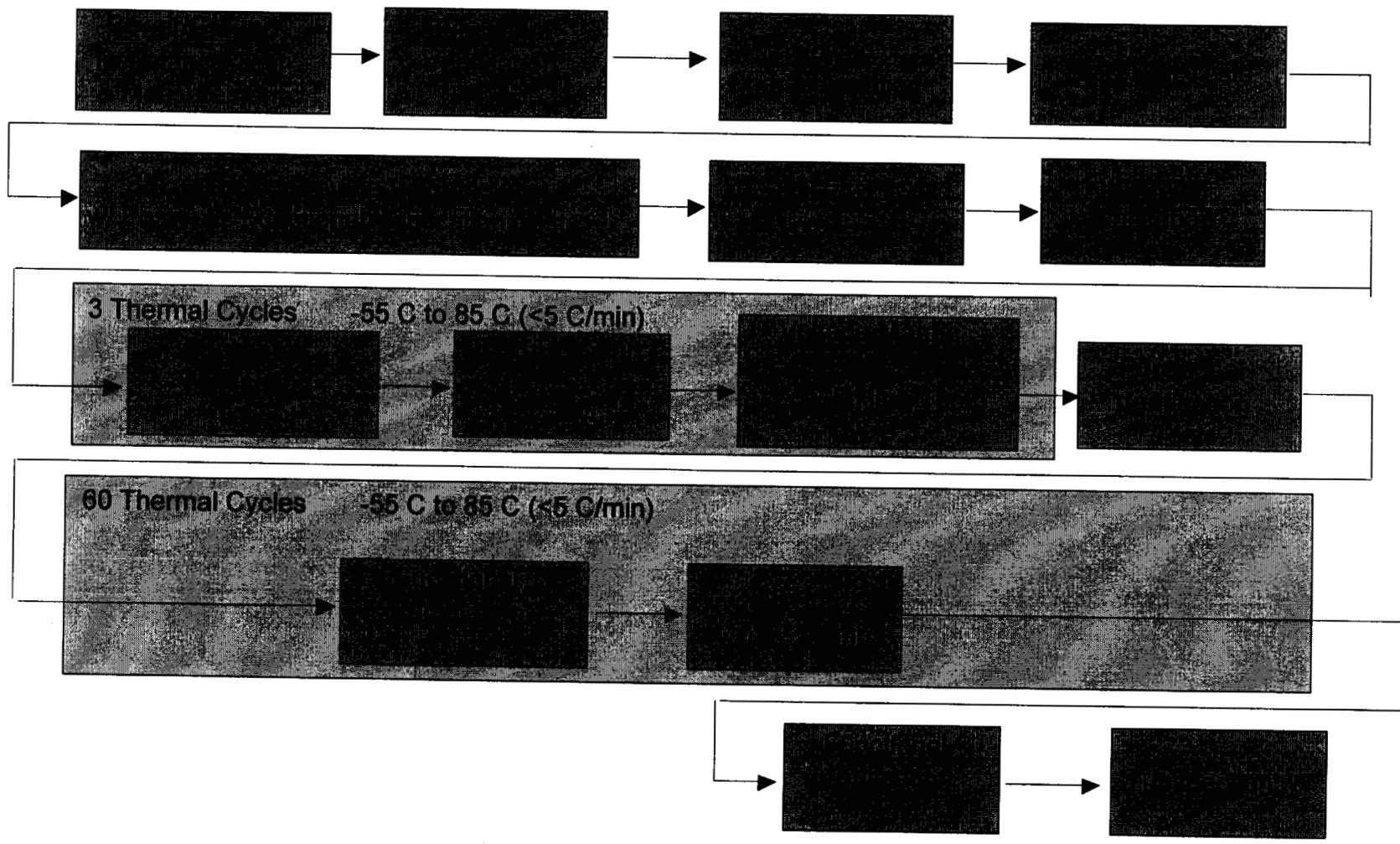
- 5x reduction in write current (now ~1.0mA)
- CMOS test chip released to fabrication, results by Q1 2002
- Array test chip in detailed designed, release projected Feb. 2002

4M/16M Chalcogenide NVRAM

- First product driven by market needs
- Built in 0.25 micron CMOS Manassas foundry
- 3.3V / 2.5V power supply
- Cycle time: $\leq 50\text{ns}$
- Write cycle endurance: $> 10^{10}$
- Read cycle endurance: unlimited
- Power:
 - Operate $\leq 10\text{ mW/MHz}$
 - Standby $\leq 50\text{ }\mu\text{W}$

Supporting Charts

SFC Qualification Test Flow - Completed



SFC Vibration Levels

Frequency (Hz)	Design/Qual, PF Test	FA Test
20-50	+9dB/Oct.	+9dB/Oct
50-250	0.20 g ² /Hz	0.10 g ² /Hz
250-350	-6dB/Oct.	-6dB/Oct.
350-1000	0.10 g ² /Hz	.05g ² /Hz
1000-2000	-12dB/Oct.	-12dB/Oct.
Overall	12.3 grms	8.7 grms

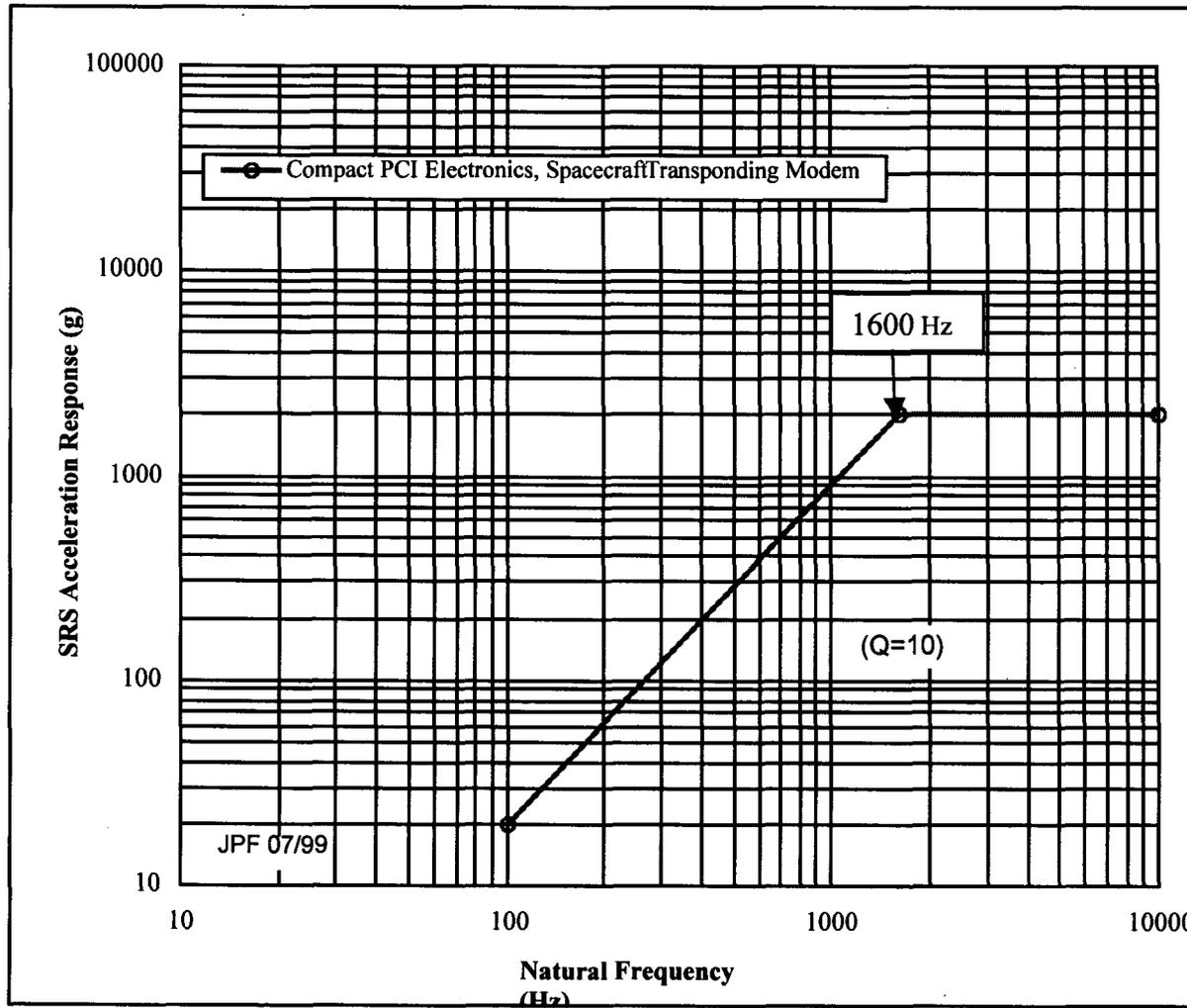
Duration: Design/Qual 3 minutes in each of 3 orthogonal axes
 PF, FA 1 minute in each of 3 orthogonal axes

Random Vibration Requirements

Frequency (Hz)	Design/Qual, PF Test	FA Test
20	1.29 g ² /Hz	0.647g ² /Hz
50-500	20.0 g ² /Hz	10.0 g ² /Hz
600-1000	10.0 g ² /Hz	5.01 g ² /Hz
2000	0.630 g ² /Hz	0.316 g ² /Hz

Random Vibration Response Limits

Pyroshock Qualification Levels



Pyroshock Design and Test Requirements

Use of RAD750™ vs. redundant commercial processors in space

Software effort and overhead

- Effort
 - Must code “upset checking” routine as well as split application code to allow for regular checking
 - Must code recovery routine
- Overhead
 - Regular output to voter chip interrupts functional processing
 - Check pointing is required more often
 - Performance loss of 50% or more is typical

SEU / SET susceptibility

- Upset mechanisms
 - Dynamic logic, found in all areas of commercial design
 - storage nodes: RAMs and registers
 - Transient (SET) propagation through combinational logic to storage nodes
- Flux rate
 - SER at 90% W.C GEO causes 1-2 upsets / hr
 - Proton projection at LEO causes 0.3-0.7 upsets / hr
 - Solar flares cause 0.1 - 20 upsets / sec
- Recovery
 - TMR recovery will typically require several minutes
 - Upsets may not be detected in

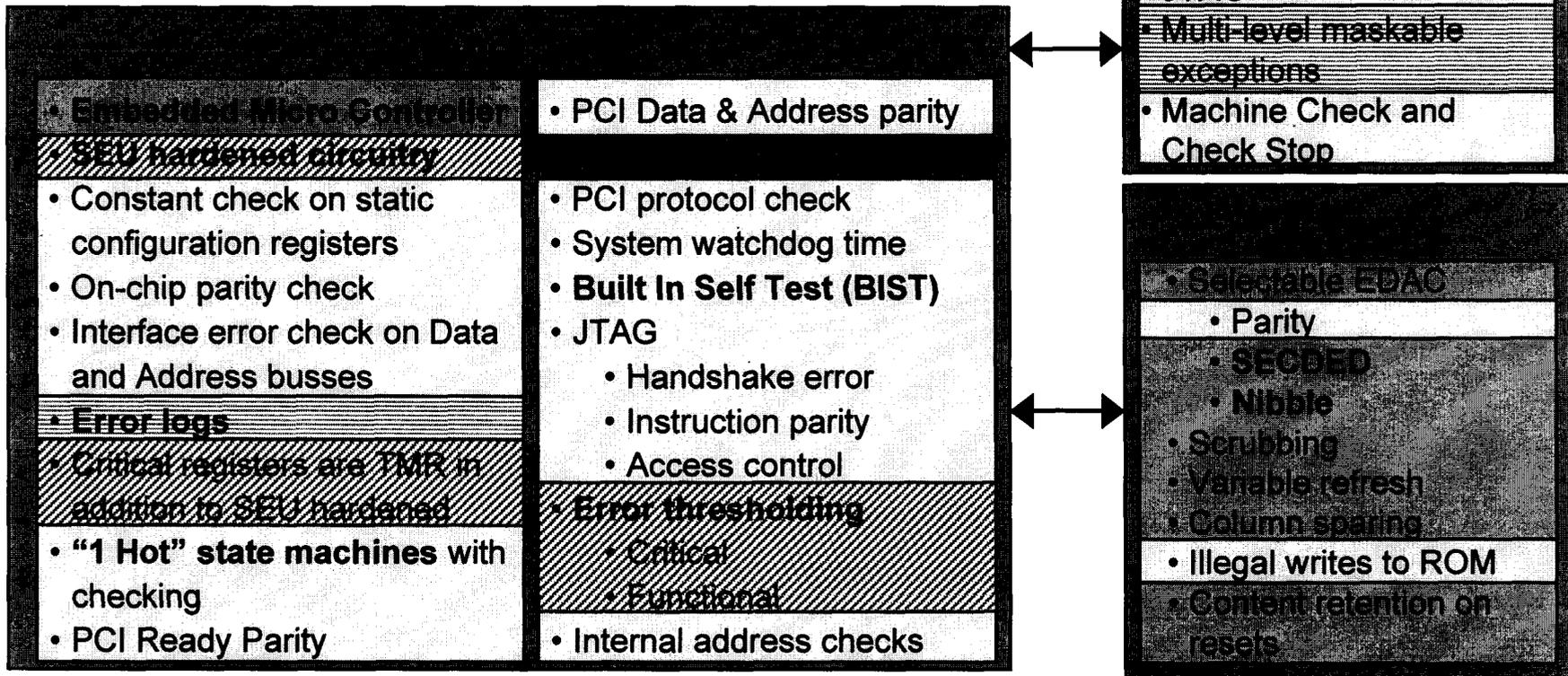
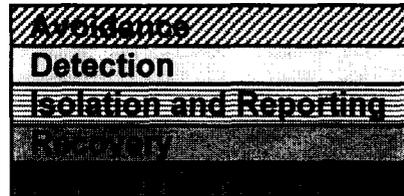
Product cost

- Component costs
 - Rad-hard voting chip has high recurring cost in addition to NRE
 - Commercial CPUs will have cost advantage
- Software costs
 - NRE for development of checking and recovery routines
- Board costs
 - More complex board design with lead time vs. a standard rad-hard product

Commercial processors, even with redundancy, have issues and exposures that far outweigh their benefits when compared to the RAD750 solution

Error detection and fault management features

Fault Tolerance Mechanisms:



The RAD750 is supplemented by the Power PCI to comprehensively address system level fault management

“The work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration.

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