TRANSFERRED SUBSTRATE HETEROJUNCTION BIPOLAR TRANSISTORS FOR MILLIMETER AND SUBMILLIMETER WAVE APPLICATIONS

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ABSTRACT

We report on our effort to develop the world's fastest transistor with the ultimate goal of utilizing them in electronic devices for advancing the present state of RF electronic systems. The approach we follow is to optimize the structure of Indium Phosphide Heterojunction Bipolar Transistors (InP HBTs), and to minimize device parasitics so that high frequency performance can be maximized. By performing a process of Transferred Substrate we are able to significantly reduce base-collector capacitance and parasitics related to the InP substrate. Presently we have demonstrated HBTs with current gain cutoff frequency (F_t) and maximum frequency of oscillation (F_{max}) of 126 and 120 GHz, respectively, in a conventional 2 μm contact lithography process without Transferred Substrate. These figures of merit are expected to improve substantially with the Transferred Substrate process and aggressive scaling of the epitaxial structure and physical geometry, which we are currently implementing. Performance enhancements of these HBTs will enable advanced high frequency amplifiers, voltage controlled oscillators, active multipliers, as well as traditional high-speed digital circuits.

INTRODUCTION AND BACKGROUND

Advancement of modern electronic systems requires improvements in their constituent components. Our goal is to progress the present state-of-the-art high-speed transistor technology, by examining their limitations, and using advance materials and methods in solving the issues. Additionally methods for manufacturability, yield and reliability are concurrently given consideration so that a feasible solution for IC enhancement can be developed.

Indium Phosphide Heterojunction Bipolar Transistors and Other Technologies

InP HBTs are one of the most prevalent high performance transistor technologies in use. The intrinsic material qualities of the family of lattice matched III-V-alloy InP HBTs allow high-speed performance with less dimensional scaling than Silicon Germanium (SiGe) HBTs. High voltage capabilities can also be designed into InP HBTs by using higher breakdown latticed matched alloys in high field regions, such as with using InP for the collectors, unlike SiGe. SiGe devices however leverage off the manufacturing technology of silicon making the technology less expensive and capable of high levels of integration. InP HBTs have recently demonstrated current gain cutoff frequency (F_t) and maximum frequency of oscillation (F_{max}) values that are comparable to or better than that of InP High Electron Mobility Transistors (InP HEMTs). Results have shown InP HBTs with F_t and F_{max} of 295 GHz [1]. Other InP HBT study report F_t of 204 GHz, and extrapolated F_{max} of 1080 GHz [2]. For InP HEMTs, F_t of 305 GHz and F_{max} of 340 GHz have been demonstrated [3]. A more recent report utilizes InP HEMTs with F_t and F_{max} of approximately 250 and 600 GHz, respectively [4]. InP HBTs achieve their high frequency performance much through device layer thickness, alloy grading and doping profile grown by molecular beam epitaxy. This is typically more

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uniformly and reproducibly done than that for InP HEMTs, which depend more on lateral scaling of the gate length by electron beam lithography for their high frequency performance. HBTs have achieved a higher level of integration than HEMTs [5]. Present studies have shown InP HBTs to have lower 1/f noise and better linear behavior making them more suitable for voltage controlled oscillators, and high linearity amplifiers. However for low noise amplifiers, InP HEMTs is the technology of choice, since it provides lower noise figures [6].

Transferred Substrate for Improving InP HBT Performance

The high-frequency figures of merit of HBTs are F_t and F_{max}. F_t and F_{max} are experimentally determined from the extrapolated frequency for current gain H_{21} and Mason's unilateral power gain (U) at 0 dB, respectively. Both H_{21} and U, as a function of frequency, are mathematically derived from S-parameter measurements. Theoretically, F_t is determined by,

$$F_t = 1/(2\cdot\pi\cdot\tau_{ec}) = 1/(2\cdot\pi\cdot(\tau_e + \tau_{cc} + \tau_f)) \quad (1)$$

Where, τ_{ec} is the total emitter through collector delay time, τ_e is the emitter charging time, τ_{cc} is the collector charging time and τ_f is the sum of the base transit times (τ_b) and collector-base space charge transit time (τ_{cd}) [7]. The maximum frequency of oscillation (power gain cutoff frequency) can be approximated by,

$$F_{max} \geq (F_t/(8\cdot\pi\cdot R_b\cdot C_{cb}))^{1/2} \quad (2)$$

Where R_b is the complete base resistance from base contact to the base layer under the emitter, and C_{cb} is the full base to collector capacitance. F_{max} can be more accurately calculated with $R_b\cdot C_{cb}$ modeled by an effective time constant of a distributed network of the base-collector region [8]. Comparing the typical mesa HBT (Fig. 1(a)) and the Transferred Substrate HBT (TSHBT) (Fig. 1(b)), the TSHBT method overcomes the limitation of the base-collector overlap in the mesa HBT since the collector contact is independently defined from the backside of the wafer. By minimizing C_{cb} - scaling in the lateral direction, F_{max} is improved. To increase both F_t and F_{max} simultaneously, scaling in the vertical direction of the base and collector to minimize transit times, and reducing the base resistance with higher doping is also required.

DEVELOPMENT OF TRANSFERRED SUBSTRATE InP HBTS AT JPL

Prof. Mark Rodwell and his group at UCSB pioneered implementation of TSHBTs. In the course of its development JPL with its specialized capabilities in electron beam lithography in collaboration with the UCSB group began submicron scaling of transistor features. Over time TSHBT performance reached a level of performance beyond other semiconductor transistor technologies (F_{max} of 1080 GHz [2]). Since utilization of TSHBTs would substantially improve electronic systems for advanced high bandwidth and high frequency applications, JPL began internally developing the TSHBT process with input from UCSB. JPL's goal is to further scale TSHBT with our new high resolution JOEL 9300FS electron beam lithography capability to further increase both F_t and F_{max}, and to improve the process for yield and

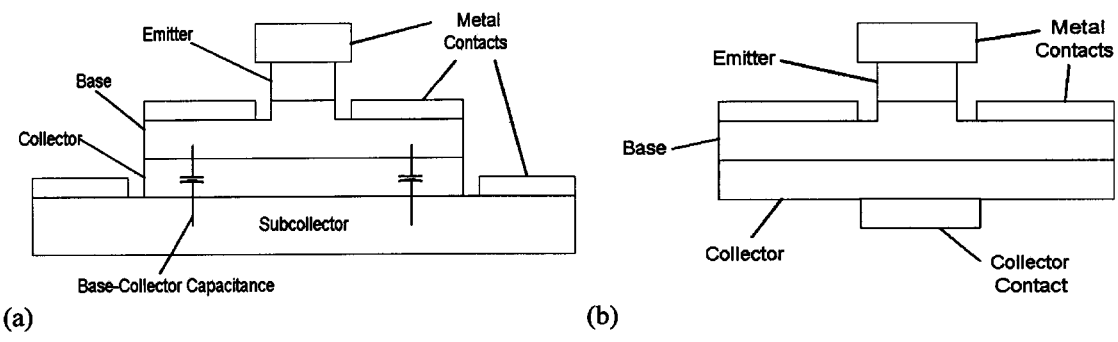


Figure 1: *(a) Schematic cross section of a typical mesa HBT. (b) Schematic cross section of a TSHBT.*

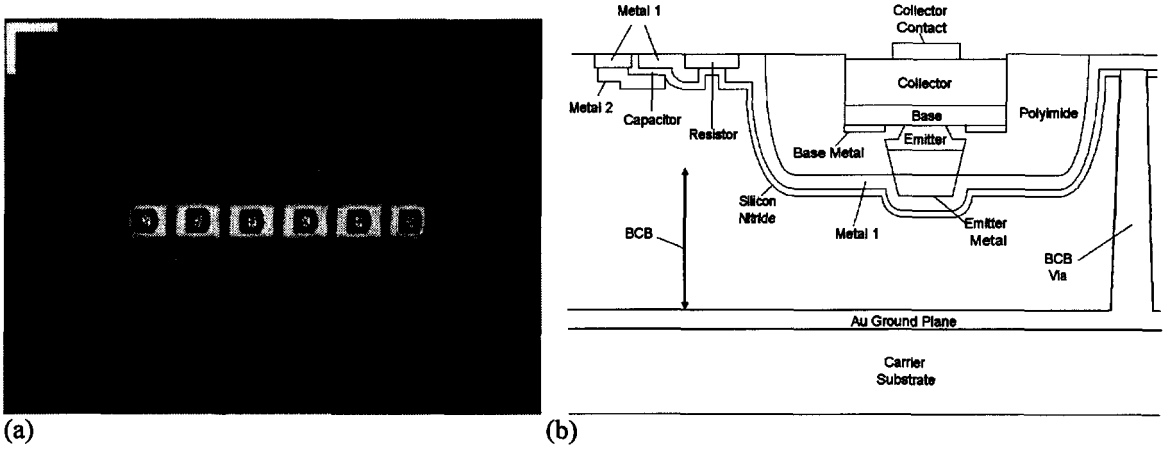
reliability, so that the technology can be used in practical applications and real systems. Extension of cutoff frequencies will directly increase operating frequencies and bandwidth of amplifiers, oscillators, and clocking rates of digital ICs. All this would benefit JPL systems by offering a faster transistor technology than is available in industry. We envision 500 GHz amplifiers and 100 GHz autocorrelators with 10 MHz resolution, which would be substantial improvements beyond current technology and enable advanced JPL instruments.

Status of TSHBTs at JPL

At JPL we are in the process of completing the first set of TSHBTs. In doing so we have gained valuable insight for the various fabrication steps, device layout and design issues that need consideration for further improvements. Figure 2 (a) shows a multi-emitter stripe power TSHBT in fabrication. Figure 2 (b) is a schematic cross section of a completed TSHBT device. The process will include on chip resistors and capacitors providing for a complete integrated process. The present TSHBT process requires 9 lithographic mask steps and 2 electron beam lithography direct writes for the emitter and collector contacts. Important in the process is the deposition of a 5 μm thick low dielectric Benzocyclobutene (BCB) resin that serves as an intermediate substrate supporting the HBTs and passive components, from the ground plane.

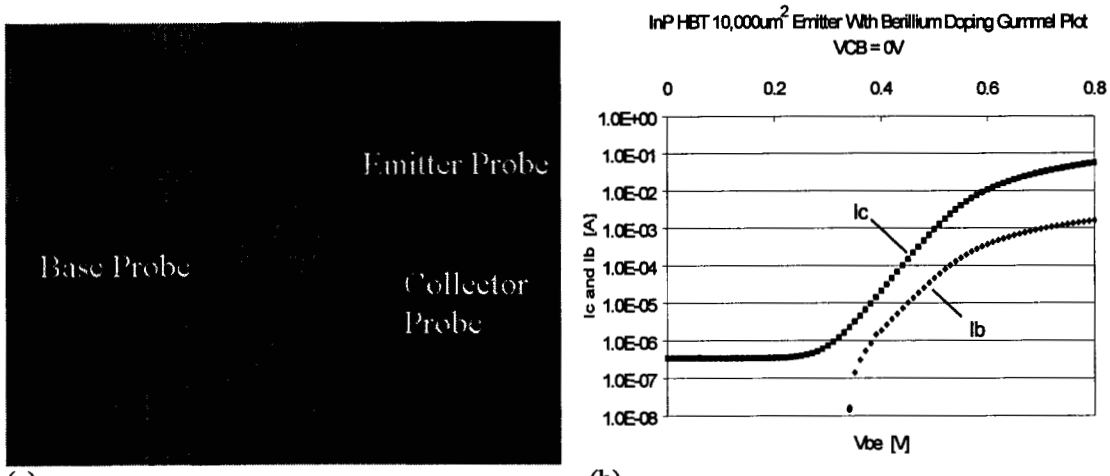
The TSHBTs process at JPL is being developed in incremental steps so that we can evaluate performance and rectify problems as soon as they are detected. In our approach, the first issue that required examination is the quality of the epitaxial wafers. Growth of the semiconductor structure is nontrivial and quality needs to be confirmed prior to taking a wafer through the entire TSHBT process. Our materials and process checks have been done in two ways. The first is to test the dc quality of the epitaxial material by making large-size HBTs in a reduced time and steps, process. Figure 3 shows a typical large sized HBT and its Gummel characteristics at a common collector-base voltage. Common emitter dc current gains (β) of 30 at an emitter current density of 0.5 kA/cm^2 are also observed.

Prior to starting the full TSHBT process, we also developed a standard mesa rf InP HBT process so that we could confirm a majority of the necessary fabrication procedures, and to examine the rf quality of the epitaxial material. The mesa rf process is common to most of the topside fabrication steps that are used in the TSHBT process. It functions as an excellent way of confirming methods towards developing TSHBTs. Figure 4 shows a completed mesa rf InP HBT with coplanar waveguides. S-parameter measurements show the InP HBTs to have F_t and F_{max} of 126 and 120 GHz, respectively. This indicates the epitaxial material and process steps are fine. At this moment we are steadily approaching TSHBT in our development and look forward in the near future to utilizing them in developing high-speed components for advancing systems.



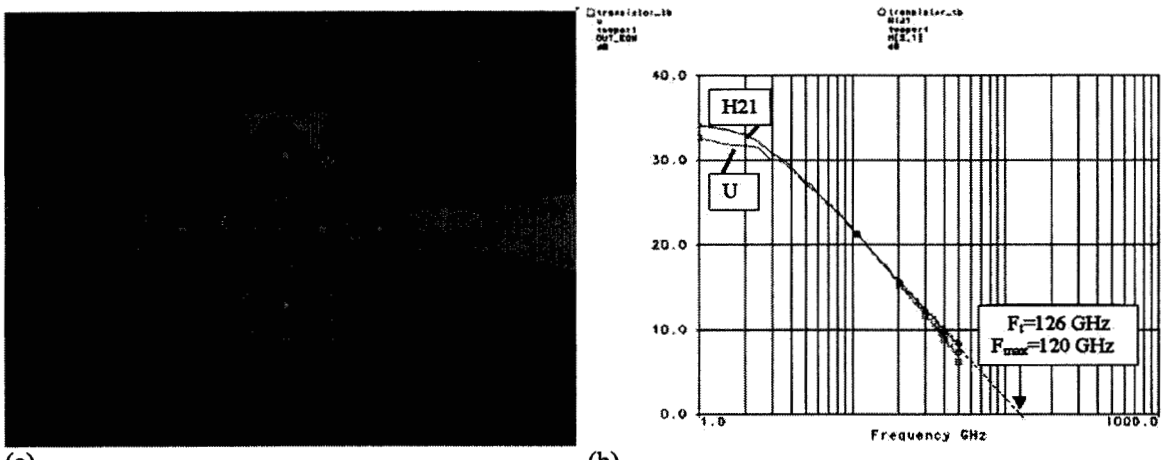
(a) (b)

Figure 2: *(a) Optical photo of a TSHBT with ballasting resistors in fabrication. (b) Schematic cross section of a TSHBT device showing integrated resistors and capacitors.*



(a) (b)

Figure 3: *(a) Optical photo of a large HBT for epitaxial materials qualification. (b) Gummel plot of a large InP HBT.*



(a) (b)

Figure 4: *(a) Optical photo of a rf InP HBT for epitaxial materials and process qualification. (b) Gain plots of a rf InP HBT deduced from S-parameter measurements. Emitter current density J_e was 62 kA/cm^2.*

Acknowledgements

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