

## **Rapid Qualification of Area Array Package Assemblies by Increase of Ramp Rates and Temperature Ranges**

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### **ABSTRACT**

Advanced area array packaging, including brought about new package technology including materials and processes as well new applications with environmental requirements not seen in their previous generation. Rapid insertion of electronics packaging technology necessitates faster qualification implementation and therefore development of accelerated test methods. Increase of ramp rate up to 20°C/min is allowed in a recently released specification, IPC 9701, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments".

Accelerated thermal cycling with a large temperature swing can be used as a environmental screening test and often has been considered as a qualification requirement for harsh environmental applications. There are many concerns, however, when such accelerations are performed especially for electronics packages with no environmental testing heritage. These concerns include: the effects of cold and hot temperatures in a cycle range, time and temperature at dwells, temperature exposure to higher than 110°C for eutectic solder, and the effects of heating/cooling rates.

A JPL-led chip scale package (CSP) Consortium of enterprises, composed of team members representing government agencies and private companies, have joined together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. The Consortium assembled fourteen different area array packages from 48 to 784 I/Os and pitches from 0.5 to 1.27 mm on multilayer FR-4 printed wiring boards (PWBs). A leaded package was used as control. In addition, two other test vehicles built by two team members, each had a control wafer level CSP package for data comparison. To meet various qualification needs of team members, assemblies were subjected to thermal cycling ranges representative of military, space, and commercial. The most rapid qualification was performed using thermal cycling in the range of 55 to 125°C with a near thermal shock ramp rates. Cycles-to-failure (CTF) test results to 3,000 cycles performed under this and three other thermal cycling ranges including 0 to 100° C are presented. The effect of ramp rate increase on CTFs and failure mechanisms for thermal cycling performed under near thermal shock and thermal cycle in the range of -55 to 125°C are also presented.