

Complementary Body Driving – A Low Voltage Analog Circuit Technique for SOI

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Abstract: This paper describes several analog circuit primitives that utilize the body terminal as a signal port. A cascode current mirror that can operate with an input and output voltage of 200 mV; and a rail-to-rail, constant transconductance gain block capable of 1 V operation are presented. These circuits have been implemented in a standard 0.35 μ m partially-depleted Silicon-on-Insulator (PDSOI) CMOS process and should find wide application in next-generation analog circuit designs.

I. INTRODUCTION

Technology scaling has enabled great advancements in the performance of both analog and digital integrated circuits. It is well known that shrinking gate lengths have increased intrinsic device speed, and lower power supply voltages have reduced the dynamic power dissipation of digital circuits. However reduced power supply voltages complicate analog circuit design because dynamic range is reduced. Current generation analog circuit designs operating at 2.5V and 3.3V routinely use wide dynamic range current mirrors and rail-to-rail transconductors [1]. However, these techniques are not applicable when the power supply voltage approaches $|V_{TP}| + |V_{TN}|$ [2].

The fundamental problem for the modern, low-voltage analog circuit designer is that threshold voltage does not scale with power supply voltage. In fact it is predicted that by 2004 power supply voltages will reach 1.0V, while threshold voltage will be as high as 0.5V [3]. Obviously circuit design techniques that are not limited to operation above $|V_{TP}| + |V_{TN}|$ must be investigated. One very promising low voltage technique is utilizing the transistor body as a signal input terminal. Body driven circuits have been successfully implemented in bulk CMOS, where a 1.0V op-amp was reported in a standard 2- μ m digital CMOS technology [4]. However a fundamental limitation of body driven circuits in bulk CMOS is that complementary devices are not available,

since the native substrate is a shared body terminal. Therefore PDSOI, which provides an isolated body contact for every device, enables complementary body driven circuits and is thus an ideal vehicle for implementing high performance, ultra-low voltage analog circuits [5].

II. DEVICE BIASING CONSIDERATIONS FOR BODY DRIVING

To enable body driving, one must first bias the gate to develop a channel inversion layer. Once the inversion layer has been formed there will be a depletion region associated with junction of the inversion layer and transistor body. The current is then modulated by varying the body voltage, which in turn modulates the inversion layer width via the depletion region. The drain current versus body voltage for this condition is described by [6]

$$I_D = \frac{\beta}{2} (V_{od0} - \gamma\sqrt{2|\phi_F| - V_{BS}} + \gamma\sqrt{2|\phi_F|})^2 \quad (1)$$

where

$$V_{od0} = V_{GS} - V_{TO} \quad (2)$$

III. LOW VOLTAGE ANALOG PRIMITIVES

A. Body Driven Cascode Current Mirror

As stated in Section I, low-voltage cascode current mirrors are commonplace in modern circuit designs. The Swoch current mirror is one popular implementation because the minimum output voltage can be as low as $2V_{DS,SAT}$ [7]. Although the Swoch current mirror finds wide application for 3.3V and 2.5V designs, it has one important limitation for ultra-low voltage operation – the input voltage must be greater than $V_T + V_{DS,SAT}$. This voltage requirement could easily be 0.75 V for the 1.0 V technology described in Section I.

Figure 1 shows a body driven cascode current mirror that is free of threshold voltage limitations, and can

therefore operate with an input and output voltage close to $V_{DS,SAT}$. Biasing of this circuit begins with setting a gate voltage so that the transistors have a conduction channel between the source and drain. Next, an input current is sourced into the drain of MN3. Note that the V_{GS} level shift onto the drains of the bottom devices forces them to be in the ohmic region, thus this circuit can also be thought of as simple current mirror degenerated by ohmic MOSFETs.

Now consider how the current mirror will operate as the input current is swept over a wide dynamic range. When the current is small MN3 will be in the ohmic region because the V_{DS} of MN3, which is equal to $I_{IN} \cdot R_{ON3}$ when MN3 is in the ohmic region, will be less than $V_{DS,SAT}$. When MN3 is in the ohmic region the feedback loop formed by the drain-body connection will have very little gain, and the current mirror will not function properly. However as the current is increased further the drain voltage will eventually reach $V_{DS,SAT}$; at this point the feedback loop will have a gain equal to

$$\text{Drain - Body Loop Gain (Sat.)} \cong \frac{g_{mb}}{2g_{ds}} \quad (3)$$

Once the transistors are biased in saturation the body driven current mirror will function just like a gate driven current mirror. If one increases the bias current further the mirror will continue to operate properly, until the body-to-source junction begins to be significantly forward-biased.

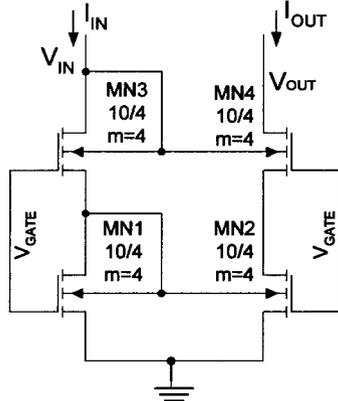


Figure 1. N-type Body Driven Cascode Current Mirror.

Figure 2 shows the measured I_{OUT} vs. V_{OUT} curves for the current mirror shown in Figure 1. All of the transistors in the current mirror are sized $(W/L) = (40/4)$, and the gate voltage for each device is set to the same fixed value. One can see in this figure that at low currents I_{IN} does not equal I_{OUT} because MN3 is not in saturation. However as the current is increased the input voltage reaches 200mV and MN3 enters the saturation region. Figure 2 shows that the current mirror operates

properly for an input voltage ranging from 200mV ($I_{IN} = 3\mu\text{A}$) to 800mV ($I_{IN} = 9\mu\text{A}$), which corresponds to a 3X current range. A method for adaptively biasing the gate to achieve operation over a wide dynamic range of currents will be the subject of future work. The measured small-signal output impedance is on the order of 10 meg-ohms.

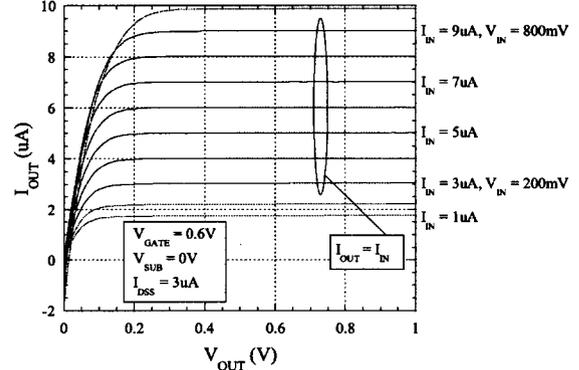


Figure 2. Measured I_{OUT} vs. V_{OUT} for the circuit shown in Figure 1.

B. Complementary Body Driven Differential Pair

Differential pairs are another critical analog building block that suffers from V_T limitations. One method of increasing the input common mode range (ICMR) of a differential pair is to employ a complementary architecture. By driving an n-type and p-type differential pair in parallel, it is possible to have an ICMR that extends to the positive and negative power supply rails. However, a complementary differential pair does not guarantee operation over the entire power supply range. In fact, when a complementary gate driven pair is used, a power supply voltage of $2V_T + 4V_{DS,SAT}$ is required for rail-to-rail operation [1]. If a power supply voltage lower than this value is used there will be a 'dead-zone' in the middle of the common-mode range where neither the PMOS or NMOS pair is turned on.

One solution to the problem of designing low voltage input stages is to employ a body driven differential pair. A body driven differential pair is one in which the gates of a differential pair are tied to a supply voltage sufficient to develop a channel inversion layer, and the input signal is applied differentially between the bodies of the transistors. In [4], it was shown that a single body driven differential pair, that is an N-type or P-type only, could provide rail-to-rail operation with a 1 V power supply; although a major limitation is that the transconductance will vary significantly over the ICMR. This transconductance variation is undesirable because important amplifier characteristics such as DC gain and

small-signal bandwidth vary proportionately with the transconductance.

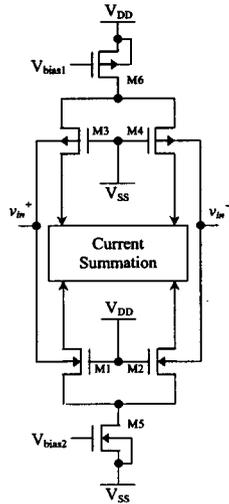


Figure 3. Complementary Body Driven Differential Pair.

In [6], it was recognized that a complementary body driven differential pair could provide rail-to-rail ICMR and constant transconductance. However the circuit described in [6] used a bulk CMOS technology, and a complementary body driven input stage was not possible. Since the technology used in this work is PDSOI, each device has its own body terminal, and a complementary body driven differential pair is realizable. A rail-to-rail, constant transconductance gain block capable of 1.0V operation is shown in Figure 3. The measured transconductance of the circuit is shown in Figure 4. This circuit achieved an average transconductance of 42 μS and varied less than 10% over the entire input common-mode range.

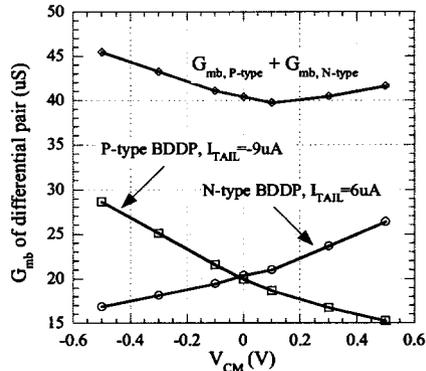


Figure 4. Measured Transconductance for Circuit Shown in Figure 3.

IV. CONCLUSIONS

This work has presented several body driven analog circuits implemented in an SOI technology. Although

body driven circuits have been described previously, this work and [5] are believed to be the first instances where complimentary body driven analog cells were presented. The advantages of complimentary body driven circuits are numerous, and include the ability to implement a 1 V rail-to-rail input stage with constant transconductance. In addition, the availability of both P-type and N-type body driven current mirrors enables the porting of traditional gate driven circuit designs directly to body driven circuit designs. It is hoped that with the information presented in the paper the reader can begin to investigate body driven circuits further. Considering the push towards lower power supply voltages, it seems very likely that body driven circuits will be an important part of next generation analog circuit designs.

V. ACKNOWLEDGEMENTS

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