

CMOS Digital Imager Design from a System-on-a-chip Perspective

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Abstract

Due to substantial mixed analog-digital circuit integration in one chip, CMOS digital imager cannot be considered only as a photoelectric transducer. In this paper, we have identified timing and circuit layout considerations that are critical for implementing a digital CMOS camera-on-a-chip. An optimized binary-scaled tree-topology power routing has been shown to be critical for minimizing chip area and providing low spatial pattern noise. Imaging artifacts due to timing asymmetry has been quantified, and methods for elimination of the artifacts have been demonstrated. The impact of on-chip bias-generation and drive circuits on the on-chip ADC performance has been shown. New timing and circuit layout techniques has been presented for enabling random noise limited performance of a CMOS imager.

1. Introduction

Over the last decade impressive advances have been made in CMOS imaging performance. Both VGA and XGA sized sensors are readily available, and larger format imagers have been built as well [1,2,3]. Advantages of CMOS imaging technology include low-cost, low-power, simple digital interface, random access, simplicity of operation (single CMOS compatible power supply), high speed, miniaturization, and smartness via on-chip CMOS processing circuits. Unlike a charge-coupled-device that is implemented in an nMOS-only technology, CMOS imagers must integrate precise analog and digital circuits - pixel array, digital timing and control processor, bias-generation and drive circuits, and analog-to-digital converters (ADCs) - all in one chip. In order to provide random noise ($\sim 100 \mu\text{V}$ r.m.s.) limited CMOS imaging performance, extreme care has to be taken for appropriate sequencing of the on-chip digital logic and layout of analog circuit blocks.

The extent of required circuit precision can be judged from the fact that the allowable leakage in an imager pixel is ~ 0.1 fA, and the pixel saturation current is of the order

of pA. In contrast, drain leakage of FETs in high performance analog and digital circuits implemented in sub-micron technologies is ~ 1 pA or higher. Thus, minute voltage and current errors resulting from inappropriate current routing, ground bounce, common-mode effects, current spikes, and capacitive coupling have enormous impact on the imaging performance. Given the regular structure of an imager, it is not surprising that any spatio-temporal asymmetry of current density around the imaging area, or any mismatch of components have a significant and visible effect on the imager performance.

In this paper, we present the digital timing, support circuit design, and power supply routing considerations required to suppress spatial noise in CMOS imagers. We present measurements carried on two large format (512^2 and 1024^2) CMOS imager-on-a-chips to highlight the problems, identify the mechanisms responsible for image degradation, and demonstrate the efficacy of alternate design methods for overcoming these problems.

2. Pixel Front End

Figure 1a shows the architecture of a CMOS digital-camera-on-a-chip. It consists of a two-dimensional pixel array, timing and control processor, ADC array, bias generation circuits, and analog and digital drivers for communicating between the on-chip analog and digital blocks. Unlike a CCD that consists of repetitive transfer of charges from the photo site to the output amplifier, a CMOS imager pixel consists of a charge-to-voltage conversion in each pixel. Figure 1b shows the front-end unit cell of the CMOS imager, along with the row line drivers. The photodetector is a reverse-biased p-n junction, that is buffered by a common-load, switched source follower comprised of M_{sf} and M_{sel} . The pixel output is a voltage available over the column bus, and can be accessed like a DRAM. The common load FET (M_{load}) located at the bottom of the column. Thus, a pixel draws current only when accessed by pulsing SEL high. The two capacitors (C_s and C_r) located at the bottom of the column are used for sampling the pixel signals. The imager operates in a column-parallel (row-wise) fashion, with each pixel being read out differentially [4]. As shown

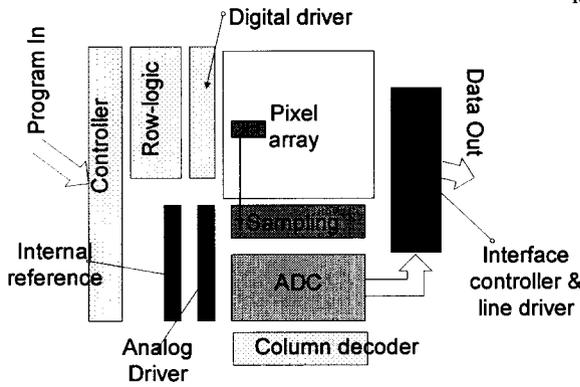


Figure 1a

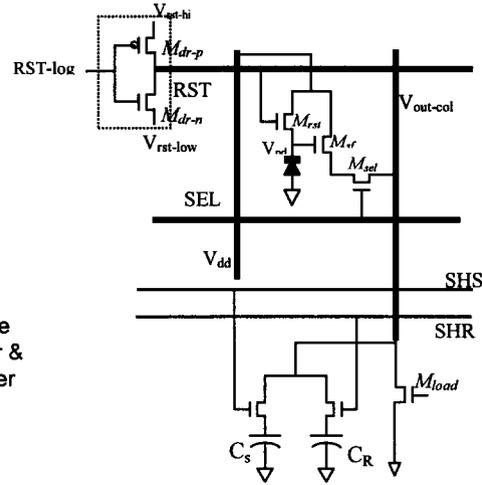


Figure 1b

Figure 1: Imager Architecture, Pixel Schematic and Pixel voltage excursion

in figure 1b, pixel reset is accomplished by driving the reset bus (RST) with the inverter line driver formed by (M_{dr-p} and M_{dr-n}). When pulsed high, RST line is driven off V_{rst-HI} .

The pixel output is generated as the difference of two measurements of the diode potential – the first value (V_{sig}) sampled prior to read-reset, and the other (V_{rstR}) following read-reset. Differential readout of the pixel enables cancellation of pixel-to-pixel offsets due to MOSFET threshold (V_T) mismatches, as well as reduction of flicker noise. The pixel is operated in a flushed-reset mode in order to eliminate signal dependent variation in the reset level for enhanced low-illumination detection ability [5].

3. Power Bus Routing

Since the reset levels are derived from the power supply, appropriate power routing is critical for high quality imaging. The chip consists of two power supplies, AV_{dd} and DV_{dd} , respectively feeding analog and digital circuits. Although they are nominally of the same value, and are tied together off-chip so that the chip operates from a single power supply, separate pads with different power supply isolation circuits are provided for the two, primarily to prevent clocking noise from corrupting internal analog signals. For the same reason, the digital logic drivers for SEL and RST signals are driven off AV_{dd} , although they are really part of the digital block. This is particularly important since analog pixel sampling lasts more than one clock cycle, while the digital logic changes state in every clock cycle.

AV_{dd} bus routing plays a critical role due to potentially large resistive drops. Although overall power dissipation in CMOS imagers is quite small, being ~ 10 - 20 mW for video-rate operation, instantaneous power draw can be

enormously large, since all pixels in a given row are activated simultaneously. For a megapixel format imager, the total current draw during pixel sampling and reset can be easily 20 mA, although each pixel draws only 20 μ A of current. The voltage drop across the power bus (i.e. maximum variation in the power supply voltage from one pixel to another) is given by:

$$V_{drop} = \frac{1}{2} \cdot N^2 \cdot I_{pix} \cdot \Omega_{sq} \frac{L_{pix}}{W_{line}} \quad (1)$$

where N is the number of pixels per row served by the power bus of width W_{line} , I_{pix} is the current flow through each pixel of length L_{pix} , and Ω_{sq} is the line resistance per square. Considering the fact that the random noise in a high performance CMOS imager is around 0.3-0.4mV r.m.s., it is desirable to have power supply matching between columns (i.e. V_{drop}) ~ 1 mV. Assuming that the power is brought to a mega-pixel pixel array from one edge, $N=1024$, and the line width needed to achieve $V_{drop} \sim 1$ mV drop is 5.2 mm for a pixel pitch of 10 μ m. A similar sized bus is needed for the ground routing as well. In comparison, the total pixel array dimensions are 10mm \times 10mm. Clearly therefore, alternate power routing schemes are necessary for proper operation of the imager.

Equation (1) indicates that the voltage drop can be significantly reduced if the number of pixels served by a power bus is reduced (due to the square law dependence). This can be achieved by using a tree-topology for power routing. The main power supply is brought from the center, and is split into equal sized branches, which are then sub-divided in the same fashion, with the width of each branch being scaled down at every stage. In this way, total width of the power bus can be reduced at the expense of somewhat increased total voltage drop across the power bus, while keeping the relative drop from one column to

another extremely small. If the power tree is designed with k branches, with the innermost branch feeding M columns, then total voltage drop (V_{tot}) from the chip pad to the edge of the column and the total width of the power bus (W_{tot}) then can be written as:

$$V_{tot} = V_{rel} \cdot \frac{\beta^k - 1}{\beta - 1}; \quad W_{tot} = W_{min} \cdot \frac{\alpha^k - 1}{\alpha - 1}; \quad \beta = \frac{4}{\alpha}; \quad (2)$$

$$N = 2^k \cdot M; \quad V_{rel} = \frac{1}{2} \cdot M^2 \cdot I_{pix} \cdot \Omega_{sq} \cdot \frac{L_{pix}}{W_{min}}$$

where V_{rel} is the maximum relative voltage drop between columns, α is the ratio by which the power bus width is increased from the innermost branch, N is the total number of columns, and W_{min} is the width of the innermost branch. Equation (3) indicates that by appropriately choosing M and W_{min} , a given V_{rel} can be achieved. Figure 2 shows dependence of V_{tot} and W_{tot} on the number of branches used for power routing. As the number of branches is increased, W_{tot} decreases while V_{tot} increases, the fractional change being dependent on α . For a given k , increasing α reduces V_{tot} , while W_{tot} increases sharply, as shown in figure 2. Since V_{tot} and W_{tot} exhibit opposing dependence on α , the optimum solution requires minimization of the product $\Phi = V_{tot} \times W_{tot}$, which requires $\alpha = 2$, indicating that the optimum routing calls for doubling the width of the power bus at each branch of the tree. Using a binary-scaled power-tree, the width of the power bus of a megapixel array biased with $20 \mu A$ of pixel current and $10 \mu m$ pixel pitch can be reduced to ~ 0.16 mm, compared to 5.2 mm. The width reduction is achieved while restricting the maximum voltage drop to < 32 mV and with better than 1 mV maximum relative voltage drop between columns. The reduced width of power bus is key to implementation of a high performance CMOS imager within an acceptable silicon real-estate.

4. Power Supply Rejection and Timing Symmetry

High frequency and low frequency variations in the power supply affect CMOS imager operation in different ways. Power supply rejection is also intimately tied up with imager timing, especially during pixel sampling, since maximum current flow occurs when a row of pixels is selected. In order to achieve variable exposure time, the CMOS camera-on-a-chip operates with a two-pointer addressing scheme, a pointer being a decoded row address [6]. The first pointer causes a row of pixels to begin integration, and the second pointer causes it to end integration, and execute a row-read sequence. The exposure time (T_{int}) is, then, determined by the temporal spacing of the integration and read pointers.

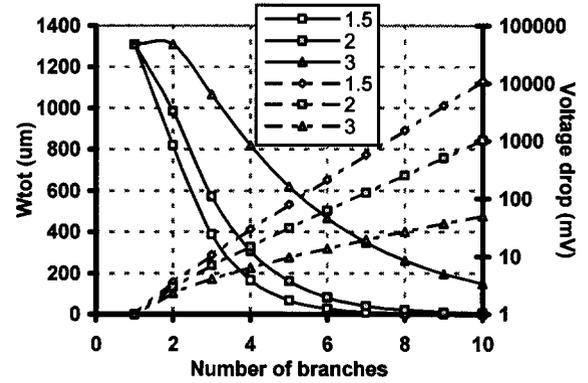


Figure 2: Total voltage drop and total power-bus width for different α values

With the pixel front-end consisting of a source-follower, the main mechanism for power supply coupling is through the modulation of the reset level, since a source-follower circuit has an inherently high power supply rejection. Thus, Reset level can be affected both by drain and gate variations on M_{rst} . Operation of an imager in “soft-reset” or in “flushed-reset” mode provides excellent immunity to M_{rst} drain voltage variations during reset, since under weak-inversion current flow, the drain potential does not affect the current flow [5]. Additionally, capacitive coupling from drain to gate is small, since $C_{gd} \ll C_{pd}$. On the other hand, V_{rst-HI} plays an important role in determining power supply rejection, since a variation at the gate of M_{rst} directly modulates the reset level on the photodiode. Row-wise spatial noise in a CMOS is directly related to the variation of the reset levels corresponding to the integration and the read pointer.

Figure 3 shows the measured AV_{dd} fluctuations during the pixel-sampling phase due to a large current draw in the chip. Although AV_{dd} spikes as much as 10 mV is observed during the reset phase, it does not affect imaging performance, as long as these fluctuations are identical in each row. However, since the captured samples are, in

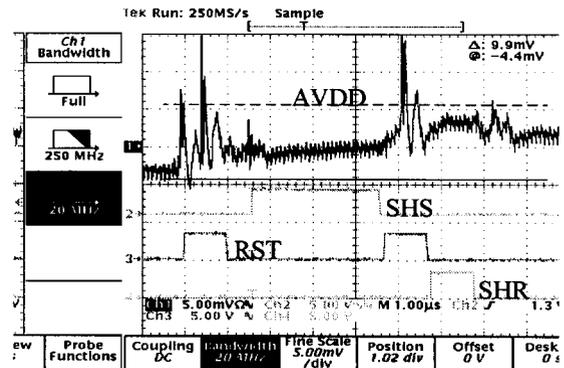


Figure 3: Power supply bounce and jitter during pixel sampling

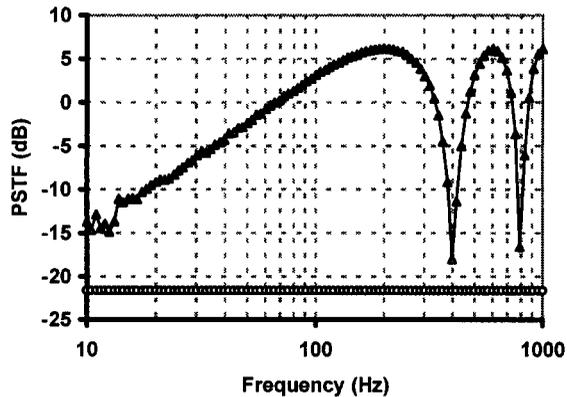


Figure 4: Power Supply Rejection Ratio (dB) as a function of Power Supply Frequency

general, uncorrelated with the power supply frequency, power supply coupling is a serious problem. Figure 4 shows the measured plot of power supply transfer function (PSTF) as a function of frequency of oscillation on the power supply. The experiment was carried out by removing all de-coupling capacitors from the power supply pads, and injecting a large 100 mV p.p. sinusoidal signal on the d.c. power supply. The imager was operated with 2.5 msec integration time. PSTF was measured by computing the spatial standard deviation within one frame, after the output of each pixel is subtracted from its corresponding dark level, allowing the measurement of the r.m.s. FPN caused by the sinusoidal excitation on AV_{dd} . The baseline flat level essentially represents the random noise floor.

As expected, figure 4 shows that PSTF is periodic with frequency, and is minimized when the inverse of the integration time is an integral multiple of the external frequency imposed on AV_{dd} . It also shows that the maximum PSTF is ~ 6 dB, corresponding to the frequency when the integration reset and the read reset occur during the opposing phases of externally imposed sine-wave. This indicates the necessity for paying close attention to low frequency decoupling of AV_{dd} , especially with respect to 60 Hz and its harmonics. Methods for the reduction of power supply coupling, include appropriate choice of exposure times (that are harmonic of the clock frequency), and separation of V_{rst-HI} from AV_{dd} and independent decoupling of both. Using these two techniques in the 512² imager, row-wise FPN was reduced below 100 μ V r.m.s. - a value lower than the random noise - rendering it insignificant.

Another problem is that internal AV_{dd} variations can occur even when the pad-level AV_{dd} is appropriately decoupled. These variations results from row-asynchronous variation in chip current density. A

variation in the current density usually stems from timing asymmetry, which is quite natural in a two-pointer mode of operation.

In two-pointer mode, a single-shot mode of operation with exposure times shorter than the frame time consists of three distinct timing states. At the beginning, only the integration pointer is active, while the read pointer is absent. Once the integrate pointer moves up a number of rows equal to the equivalent exposure time, both read and integrate pointers become active, although they point to different rows. Finally, only the read pointer is active. In the video-mode, except for a dead-time interval inserted to maintain a minimum exposure time equal to one row time, both pointers are always active. During the time period a pointer is inactive, no SEL signal is generated, and no current is drawn by the pixel source-followers. As a result, internal AV_{dd} changes due to an absence of any IR drop. The variation of AV_{dd} due to the absence of one of the pointers causes V_{rstI} and V_{rstR} to be different, resulting in a pixel d.c. offset that depends upon which of the three states the imaging chip is in.

Figure 5 shows the impact of timing asymmetry on the row fixed pattern noise and the associated imaging artifact. Figure 5a shows the flat-field voltage distribution and the row-gradient with the imager held in dark, and operated in a single-shot mode. Three distinct d.c. level regions can be clearly seen, corresponding to the presence or absence of integration and read pointers. Depending upon the exposure time, the location of these zones will shift temporally, with the lowest offset condition corresponding to the situation when both pointers are active, resulting in a locally uniform current density. It

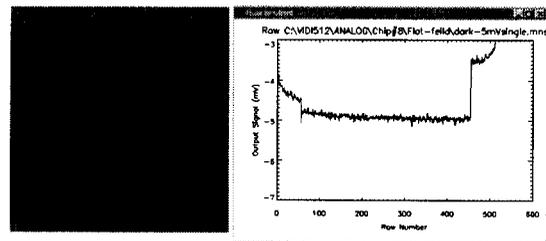


Figure 5a: 1-shot: 5 mV mean signal

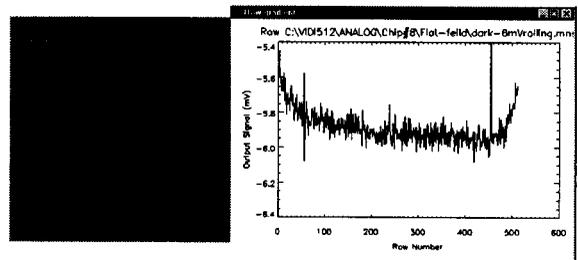


Figure 5b: video: 6 mV mean signal

Figure 5: Timing asymmetry and its impact on the imaging performance

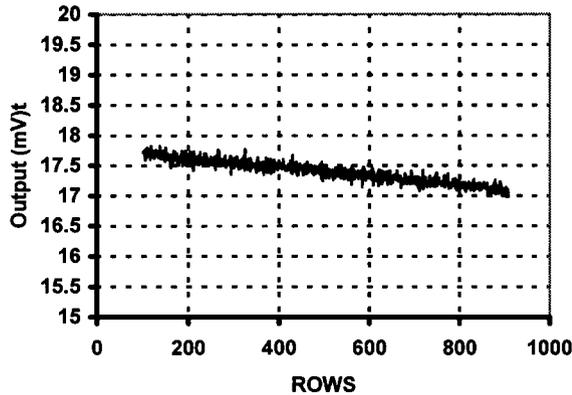


Figure 6: Row-cross-section for the megapixel imager with symmetric timing

must be noted that although the error due to timing asymmetry is only ~ 2 mV, it is significant from the standpoint of maintaining high imaging performance, since it corresponds to 4 times the random noise level, and is clearly visible. Figure 5b depicts the video-mode of operation. In this case, the timing asymmetry is present only during the dead-time, and hence appears as a spike, or visually as a “hot-row”.

Fortunately, this error can be easily corrected by selecting a dummy row anytime one of the pointers are absent, thereby ensuring a constant current density. Measured data from the megapixel imager, implemented with this approach, shows that the “hot-row” has been eliminated, as can be observed from the row FPN data shown in figure 6.

5. Analog-To-Digital Converter (ADC)

Low-power imaging requires digitization of photo-generated signals as close to the pixels as possible in order to eliminate the high power consuming driver amplifiers. A column-parallel ADC architecture, where the analog output from each column is connected to its own ADC, is used for digitization. The parallelism in this architecture enables minimization of power without sacrificing data rates, by allowing individual ADCs to operate at much lower speeds. Only a 100 kHz conversion rate is required for a 1024^2 imager operating at video rate.

For ultra-low-power digitization, an all-capacitor successive-approximation ADC (SA-ADC) algorithm is implemented [7]. Successive binary-scaled references, required the SA-ADC algorithm, are generated with binary scaled capacitors. Binary decimation of the reference required in each cycle is accomplished by pulsing the bottom plate of a bit cell capacitor C_i to V_{ref} , raising the voltage on C_s by the capacitive divider ratio or

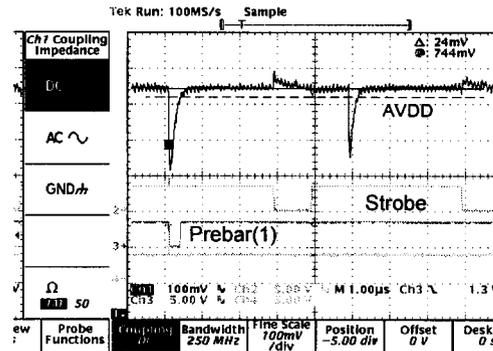


Figure 7: Power supply bounce and jitter during ADC operation (the sharp drop occurs during binary scaled reference generation)

equal to $V_{ref}/2^i$. An on-chip bias generation and analog driver circuit provides V_{ref} . By digitizing the difference between the pixel reset and signal levels (V_R and V_S), the digitized value is made inherently immune pixel threshold mismatches. An additional calibration phase is used to cancel the offset generated by the comparators and internal buffer circuits. Pseudo common-centroiding of the top most significant bit capacitors is used to minimize matching errors. Similarly, the capacitors are designed as multiple blocks of unit cells with proportionally same edge and parasitic capacitance.

Due to parallelism, total capacitance of all ADC's is large, being around 4 nF. With the capacitors operating in a pulsed-mode, stable reference (V_{ref}) generation poses major challenges. Figure 7 illustrates the problem of limited output impedance of the on-chip reference driver. The dip in AV_{dd} caused by the need for instantaneous charge supply from the power bus when the bottom plate of the capacitors are swung, settles back with a finite time constant. If the driver impedance is not low enough to sufficiently settle within a small time (~ 500 nsec) available prior to comparator triggering, the comparator makes an erroneous decision, resulting in additional differential non-linearity (DNL) at that bit.

Figure 8a and 8b shows the DNL of the on-chip ADC, with the V_{ref} driven from high and low impedance drivers. With a high impedance driver, (figure 8a) V_{ref} does not sufficiently settle prior to comparator triggering, and it results in significantly increased DNL. The DNL is also noticeably worse for higher codes than for lower. This results from the fact that for codes above 512, more capacitors have their bottom plates tied to the noisy V_{ref} rather than to the low-noise ground. This exacerbates the settling problem. Figure 8b shows that by increasing V_{ref} stability through the use of a low-impedance driver, significant improvement in DNL can be achieved, allowing digitization with $DNL < 0.5$ LSB. A summary of the relevant imager performance parameters is provided in

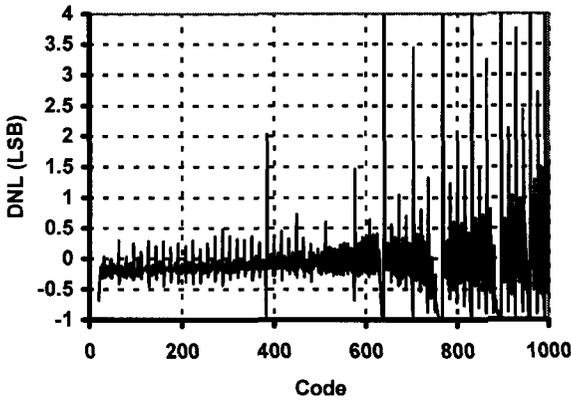


Figure 8a

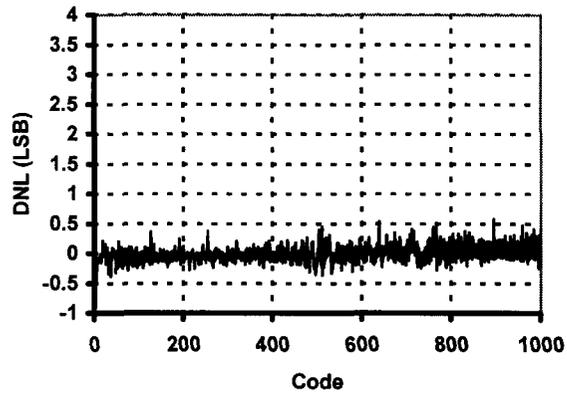


Figure 8b

Figure 8: Differential non-linearity of ADC for improper V_{ref} driver design

table 1. It indicates that spatial noise due to timing and circuit layout has been reduced below the read noise floor.

6. Conclusion

In summary, we have identified timing and circuit layout considerations that are critical for implementing a high performance digital CMOS camera-on-a-chip. It has been shown that power supply routing plays a critical role, and binary-scaled tree-topology power routing represents an optimum power routing scheme that reduces the bus width to acceptable values, while obtaining column-to-column supply matching to better than 1 mV. Imaging artifacts due to timing asymmetry has been quantified, and methods for elimination of the artifacts have been demonstrated. Finally, the impact of on-chip bias-generation and drive circuits on the on-chip ADC performance has been shown. These effects demonstrate the importance of approaching the design of a digital

Table 1: Relevant CMOS Imager Characteristics

| Imager characteristics | Values | Comments |
|------------------------|------------------------|---------------------------------|
| PSRR | -6 dB min 22 dB max | Max. corresponds to noise floor |
| Row pattern noise | 2 mV 0.1 mV | With and w/o timing asymmetry |
| Column pattern noise | 0.25 mV | |
| Random Noise | 0.45 mV | |
| DNL | 4 LSB 0.5 LSB | W/ and w/o V_{ref} bounce |
| Gain variation | < 1% | Across the array |
| Data Rate | 20 FPS | W/10 MHz clock |

CMOS imager within the system-on-a-chip paradigm. Appropriate timing and circuit layout has been shown to be critical for suppression of spatial pattern noise effects, enabling random noise limited imager performance.

7. Acknowledgements

The research described here was performed by the Jet Propulsion Laboratory, California Institute of Technology, and was funded by the National Aeronautics and Space Administration, Office of Space Sciences.

8. References

- [1] S. Inoue et al., "A 3.25 megapixel APS-C size CMOS imager", *Proc. IEEE Workshop on CCD and Advanced Image Sensors*, pp. 16-19, 2001.
- [2] A. Krymski et al., "A high-speed, 240 frames/sec 4 Megapixel CMOS imager", *Proc. IEEE Workshop on CCD and Advanced Image Sensors*, pp. 28-31, 2001.
- [3] M. Loose et al., "2/3" CMOS imaging sensor for high-definition television", *Proc. IEEE Workshop on CCD and Advanced Image Sensors*, pp. 44-47, 2001.
- [4] S. Mendis et al., "CMOS active pixel image sensors for highly integrated imaging systems", *IEEE J. of Solid-state Circuits*, vol. 32 (2), pp. 187-198, 1997.
- [5] B. Pain et al., "Analysis and enhancement of low-light-level performance of photodiode-type CMOS active pixel imagers operated with sub-threshold reset", in *Proc. IEEE Workshop on CCD and Advanced Imager Workshop*, paper R-13, 1999.
- [6] B. Pain et al., "One chip digital camera with extended low-light detection capability", in *Proc. 2000 13th. VLSI Design Conference*, pp. 342-349, 2000.
- [7] Z. Zhou et al., "CMOS active pixel sensor with on-chip successive approximation analog-to-digital converter", *IEEE Trans. on Electron Devices*, vol. ED-44, pp. 1759-1763, 1997.