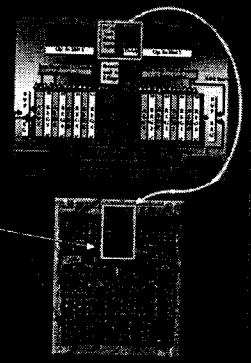
HTMT

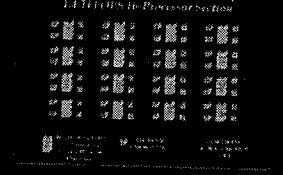
SCE PROCESSOR ARCHITECTURE

FLUX-1 Communication-Aware Architecture

- A partitioned architecture requiring short-distance interaction and reduced connectivity between processing and storage elements
  - interleaved arithmetic-logic units (ALUs) and registers
- Using regular structures
  - a 2-dimensional datapath built with simple building blocks
- Merging related structures
  - PC & instruction select logic & memory address decoder



Scalable Non-Uniform Memory Access SuperPro L4 TFLOPS 16-Processor Section



PETAFLOPS SYSTEM

2009

SPELL

- 16 Multi-Stream Units
- 8 Strands / MSU
- 50 GHz or higher clock speed
- 250 GFLOPS @ 50 GHz
- 300 - 400 K gates

- *SuperPro system*
- 32 64-bit multithreaded vector processors
- 30 GHz clock
- 1MB+ L1 SC memory/processor
- High-throughput Xbar switch(es)
- 500K+ logic gates/chip
- 90 Gflops / processor (peak)
- High-speed I/O
- ~ 2.8 Teraflops / system (peak)

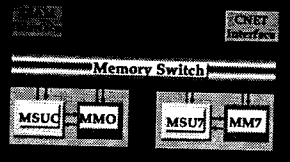
- *FLUX-1: Technology demonstration*
- 20 GHz
- 6K logic gates / chip
- 1 chip / MCM

2002

- *FLUX-2: Multi-chip assembly w/ 32-bit FP computing on vector registers*
- 25 GHz clock
- ~10K gates / chip
- 4 Kbits / FIFO memory chip
- 3 chips / MCM
- 25 GHz chip-to-chip data rate

- *SuperPro MCM*
- *32/64-bit multi-chip processor with L1 SC memory*
- 25 GHz clock
- 60 Gflops/processor
- 50-100K logic gates / chip
- 64 Kbits / memory chip
- 10+ chips / MCM
- High speed I/O ports

SPELL-1 Multithreaded Processors for Petaflops Computing



SPELL-1: an 8-node multiprocessor with simultaneous multithreading and distributed shared pipelined L1 superconductor memory

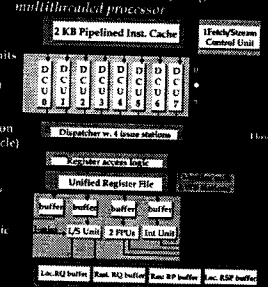
Multistream Unit (MSU): an 8-way fine-grain multithreaded processor

8 Decode / Control Units with in-order single-instruction issue from each stream

Out-of-order instruction completion (4 inst / cycle)

4 64-bit Units: Load / Store, Integer, FP Add, and FP Mlt

Memory Interface Logic



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