

# EEPROM Bit Failure Investigation

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## *Abstract*

This paper reports the investigation findings concerning of the EEPROM single bit failures that were observed on a recent NASA space mission. We have concluded that "weak cells", due to either process-induced defects or poor programming, may be the root cause. Reliability analysis was performed along with a diagnostic and write/read cycle testing, which was designed to emulate "weak cells" and to study their data retention characteristics and estimate their activation energy. We have also concluded that the EEPROM is very sensitive to program timing. Board timing and noise margins need to be extensively analyzed to avoid possible weak cells induced by inappropriate programming, which in turn may result in early bit failures.

## I. INTRODUCTION

A recent NASA space mission reported two EEPROM single bit failures. One failure was observed approximately six months into flight and the second bit failure followed seven months later. The two bit failures were located in the same physical Multiple Chip Module (MCM) package but different dies. In both cases, the contents changed from "0" to "1", i.e. from a charged state to a discharged state.

This work is to investigate the possible root cause(s) for the two bit failures observed. Section II provides a reliability analysis of the EEPROM bit failures under different operating conditions based on the EEPROM data sheet and reliability report provided by the EEPROM manufacturer. Section III gives a detailed investigation on weak cells performed on the EEPROM chips from the same manufacturer. Summary and conclusions of this investigation are included in section IV.

## II. RELIABILITY ANALYSIS

Data retention characteristics degrade over temperature and erase/write cycles. Endurance refers to the number of erase/write cycles before read errors develop, which is the wear-out mechanism due to write/erase cycles, and therefore is also a function of temperature and erase/write cycles. The data sheet and reliability report by the EEPROM manufacturer shows a 10X degradation of data retention after 10,000 erase/write cycles versus no erase/write cycle. To date, since the mission observing the two bit failures has undergone approximately 10 erase/write cycles and the two bit failures changed from a "0" (charged state) to a "1" (discharged state), data retention resulting from cell discharge appears to be the cause of failures.

Data retention failures resulting from faster cell discharge can be caused by high temperature operation, excessive read cycles, radiation or/and "weak cells", which will be discussed one by one in this section.

### *A. High Temperature Operation*

High temperature can dramatically accelerate the cell discharging process and therefore EEPROM operated under higher temperature conditions is susceptible to a much shorter lifetime of data retention. Based on the EEPROM data sheet and reliability reports provided by the EEPROM manufacturer [1], the data retention characteristic can be calculated as a function of operating temperature.

Figure 1 shows the number of EEPROM chip failures per million EEPROM chips versus years in operation at temperatures of 30°C, 40°C, 50°C, 60°C and 70°C. In this case, EEPROM chip failure is defined as the first data retention bit

failure on the chip. The estimated operating temperature for the mission observing the two bit failures is around 55°C and according to Figure 1, an EEPROM data retention bit failure should not be expected within the first seven years of operation under 55°C. In addition, since two other NASA missions are operating the same parts under higher temperature (~70°C) conditions without experiencing data retention bit failures, higher temperature operation alone in this case is not considered as the root cause of the bit failures observed on the mission.

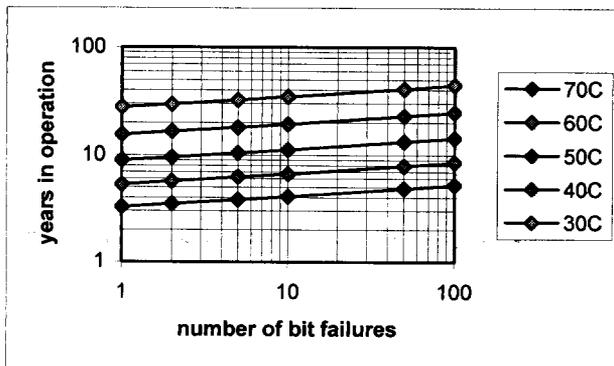


Figure 1. The number of EEPROM bit data retention failures vs. years in operation as a function of temperature.

### B. Excessive Read Cycles

Read voltage required is much lower than write voltage. Write cycles cause high-energy electrons to pass through and generate traps in oxide/nitride film. This will degrade the quality of the dielectric film and reduce the difference between the threshold voltages of “1” and “0” states. Read cycles can also contribute to cell discharging degradation but its impact is much smaller unless excessive read cycles are performed on weak cells. There is no existing information on read cycle induced data retention characteristics from the EEPROM data sheet or reliability report provided by the manufacturer. In order to provide recommendations on CRC, the read cycle impact is included in our investigation, which will be described in section III.

### C. Radiation

The EEPROM is fabricated using MNOS technology. MNOS technology has typical robustness for a commercial part, i.e. the peripheral CMOS has a TID limit of 30 krad(Si), the charge pump used in write commands has a limit of 7

krad(Si), and the MNOS array is robust to a TID well in excess of 100 krad(Si) [2]. Based on the fact that, up to date, the mission observing the two bit failures has less than a 2krad total dose exposure, it is concluded that total dose is not considered to be the cause of the bit failures on the mission.

Concerning anomalous charge loss from a single bit from a heavy ion strike, Blandford et al. demonstrated that no errors occur in a properly programmed MNOS device after exposure to over  $1e7 \text{ cm}^{-2}$  ions of high LET ions [3]. Given that the total fluence of particles capable of inducing a bit error at 2krad(Si) is approximately  $1e4 \text{ cm}^{-2}$ , it has also concluded that heavy ion strike can be effectively excluded from the mechanism of an anomalous charge loss event on the mission.

### D. “Weak Cells”

“Weak cells” refer to any memory cell whose reliability behavior is not related to its structural, functional or material properties. In other words, the reliability characteristics of “weak cells” are of extrinsic nature. “Weak cells” can be induced by process and/or poor timing and/or noise margin during programming.

Process-induced weak cells can be defective cells resulting from defective oxide, oxide thinning, oxide excessive trapping, abnormal leakage path through silicon or oxide, adjacent via bridging, adjacent metal bridging, metal flake, metal void, etc. As a result, these weak cells cannot hold as much charge, or for as long as nominal cells.

Errors in timing margin during programming can also induce weak cells. In this case, the cell may either have lower write voltage or shorter write time, which results in less charge stored in the cell and therefore, a shorter data retention life expectancy.

Weak cells may have several orders of magnitude lower data retention lifetimes and a much higher failure rate. Although the basics of failure mechanisms for weak cells are the same as those of nominal cells, the activation energy may

be much lower and therefore, weak cells are more susceptible to failure during high temperature operation.

The data retention characteristics from the EEPROM data sheet and reliability report provided by the manufacturer are for intrinsic EEPROM chips and cells and cannot explain or project the lifetime or failure rate for weak cells. Figure 1 shows that an *intrinsic* EEPROM data retention bit failure should not be expected within the first five years of operation under operating condition of 50°C to 60°C. An *extrinsic* bit failure resulting from a *weak cell* can happen at any time before the intrinsic bit failure occurs. Based on the above analysis, radiation, high temperature operation, and excessive read cycles have been excluded as causes of the failures on the mission observing the two bit failures. Weak cells, either induced by process or poor programming, are likely to be the root cause.

### III. DIAGNOSTIC TEST TO EMULATE WEAK CELLS

In order to investigate the reliability characteristics and obtain the activation energy of the weak cells, a diagnostic and write/read cycle testing plan was developed to emulate the weak cells by externally modulating the write voltage. The experiment was performed on EEPROM chips from the same manufacturer.

#### A. Modulating Write Voltage to Emulate Weak Cells

The EEPROM parts under investigation were inspected optically before application of electrical testing. The chips were packaged in a 32-pin configuration but were observed to have 33 bond pad contacts on each chip. One of the bond pads is a spare that is not connected to the exterior of the package. The pad was traced directly to the charge pump structure.

Diagnostic and write/read cycle tests were designed to investigate the single bit failure mode by modulating the voltage on the spare bond pad. This was used to study a weakly programmed array of EEPROM bits. A partially programmed array was postulated to exhibit early bit failures similar to the bit failures observed on the mission.

Partially programmed cells will hold less charge and therefore, exhibit reduced data retention properties, i.e. early bit errors and lower activation energy. This method of partially programming the device used the spare pad on the die that was related to the charge pump.

The charge pump pad was measured to be 0 volts during idle and read operation. During the write operation the pad was measured at -4V on the EEPROM device under test (DUT). Using a microprobe and a pull up resistor, the voltage on the pad was modulated during the write operation. This demonstrates that the voltage potential on the spare bond pad is related to charge pump bias and therefore, by changing the voltage potential on the spare bond pad externally, write voltage on the cells can be adjusted. Using this method, the programming voltage could be modulated during a write and, therefore, the charge in the EEPROM cell could be modulated.

Figure 2 shows the number of write cycles needed to program a DUT so that no read-after-write errors were reported as a function of the programming bond pad voltage. Two parts were tested and exhibited a similar trend of requiring more write commands so that no errors are reported during a read as the bond pad voltage was increased. The fact that this characteristic is almost the same for two parts, shown in Figure 2, indicates that the voltage is intrinsic to the chip and so modulating this potential to change cell performance can be representative of all arrays.

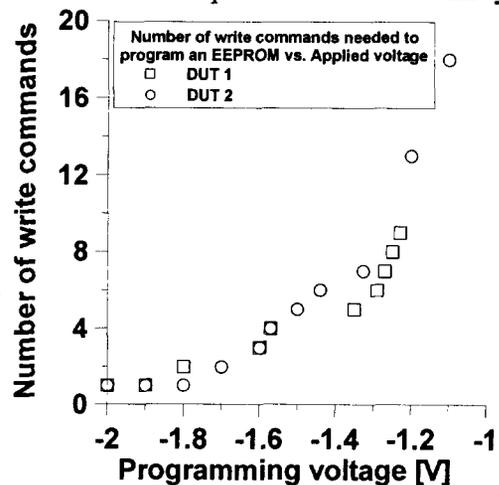


Figure 2. Number of write cycle as a function of the modulation voltage on the spare bond pad for two EEPROM parts.

### B. Impact of Read Cycles on Weak Cells

Once a DUT is programmed in the manner demonstrated in Figure 2, the relative strength of programming voltage operations can be compared. The impact of read cycles on the data retention characteristics can be seen in Figure 3, where the number of read cycles that occur before an error is reported is plotted as a function of the bond pad voltage on the spare bond pad. The experiment was performed on an Advantest that read the part at a frequency of 15000 per second. For fully programmed cells, we did not observe any error before at least  $5 \times 10^9$  read cycles.

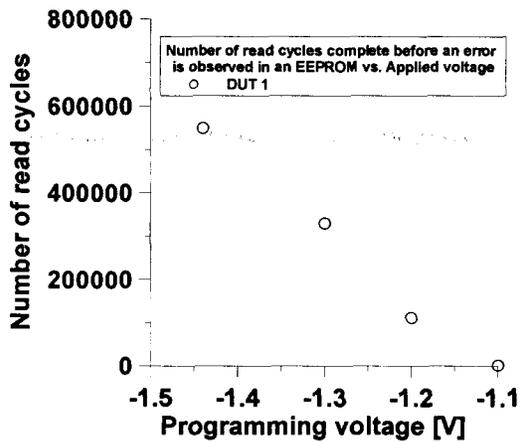


Figure 3. Number of read cycle as a function of the modulation voltage on the spare bond pad.

Figure 4 details the growth of bit errors on the DUT when read continuously at  $1.5 \times 10^4$  device reads per second. The device was programmed with the voltage potential at the spare bond pad as a  $-1.2\text{V}$ . It shows error growth as a function of elapsed time, translated from the readout frequency of  $1.5 \times 10^4$  DUT readouts per second.

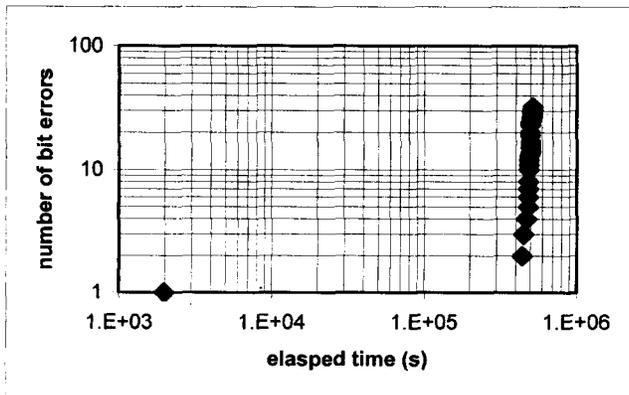


Figure 4. Number of bit error as a function of elapsed time when the modulation voltage on the spare bond pad is  $-1.2\text{V}$ .

The data retention characteristics of weakened cells are a function of time. Time after programming, therefore, may be the variable that controls the error growth rate and not the number of read cycles. To determine the relative contribution to readout frequency on error rate, error growth rate was observed for two different DUT readout frequencies,  $1.5 \times 10^4$  DUT readouts per second and 1 DUT readout per second. Reducing the frequency of the readouts effectively reduces the effect of any electric fields in the array so that the charge removal is due mostly to diffusion in the oxide. This experiment is intended to separate the drift and diffusion components of the charge removal mechanism from the oxide.

Figure 5 demonstrates the effect that readout frequency has on data retention. Two tests were performed at  $1.5 \times 10^4$  readouts per second and one test was done at one readout per second. Figure 5a plots the number of errors as a function of elapsed time. Figure 5b plots the same data converted to readout cycles after programming. Data from the two  $1.5 \times 10^4$  readouts per second tests demonstrate good repeatability. The data exhibit the following three characteristics:

- The failure time of the first error does not change significantly for either readout case as shown in Figure 5a. Both the  $1.5 \times 10^4$  reads per second test and the one read per second test experience the first failure at approximately the same time. This constancy implies that the electric field present during readout does not significantly affect the time it takes to report the first error. It also indicates that the first error is predominantly driven by the data retention characteristics of the EEPROM, and the electric fields present during a read operation have a secondary effect.
- The frequency of device reads does have an effect on the rate of error growth. After the first bit error, the read frequency test at  $1.5 \times 10^4$  reads per second yields faster error growth per unit time than the one read per second test. This effect implies that reading more often will accelerate bit error growth

of weakened cells for the same data retention time.

- c. The address location for each failure was different, which indicates that this is a statistical phenomenon intrinsic to the cells.

However, it should be pointed out that the data sets acquired in this study do not quantify the relative strengths of the effects due to small statistics.

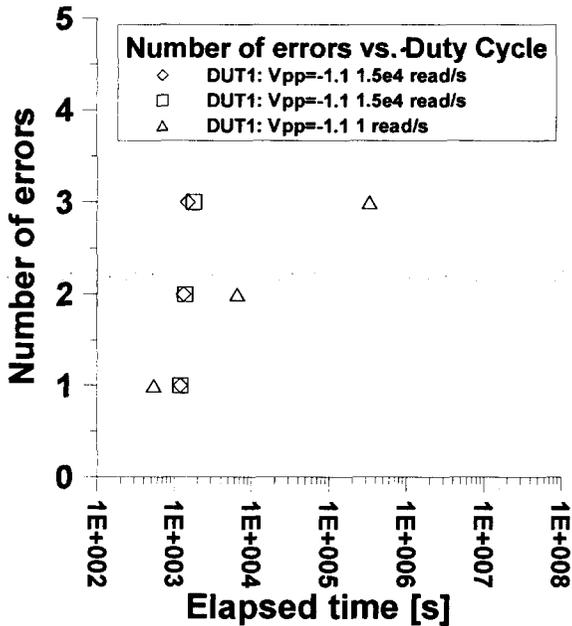


Figure 5a. Number of bit error as a function of elapsed time when the modulation voltage on the spare bond pad is -1.1V.

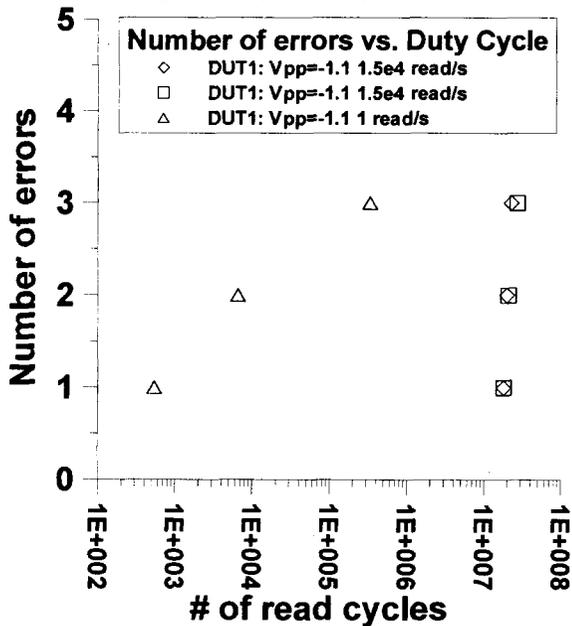


Figure 5b. Number of bit error as a function of elapsed time when the modulation voltage on the spare bond pad is -1.1V.

The activation energy for data retention from the manufacturer's reliability report is cited as 1.1eV. This activation energy is believed to be the activation energy for data retention of intrinsic memory cells. The activation energy for extrinsic cells, or weak cells, may be different from, and in most cases, smaller than this value and depends on which mechanism(s) are associated with the formation of the weak cells. The DUT programmed at reduced charge pump bias -1.2V was tested at 27°C and 85°C to obtain an estimate of the range of activation energy for those poorly programmed weak cells. The results are shown in Figure 6. The activation energy was estimated around 0.5eV to 0.7eV, which is less than the 1.1eV for intrinsic cells and therefore can be more easily thermally activated to discharging than intrinsic cells.

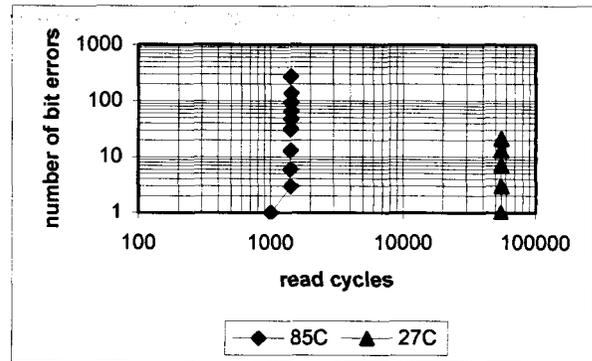


Figure 6. Number of bit failures as a function of read cycles on DUT1 at 27°C and 85°C for activation energy estimate.

### C. Programming

During the investigation, additional EEPROM bit failures were observed on two ground system boards. Figure 7 provides the waveform characteristics of the failing bit. However, using both Advantest and PCI interface bus, the two single bit failures at board level could not be confirmed.

This inconsistency indicates that the single bit errors may also be due to board level related program timing or noise margins. One example for this EEPROM part is when the write time is less than 100ns and/or hold time is less than 10ns before performing read-after-write operations. Errors in noise margin can also cause weak cells. One case is when the noise pulse width on the control pins is over 20ns during read and standby

mode, which may act as a trigger to return the device to programming mode. Therefore, board timing and noise margins during programming needs to be carefully analyzed to prevent possible EEPROM bit failures.

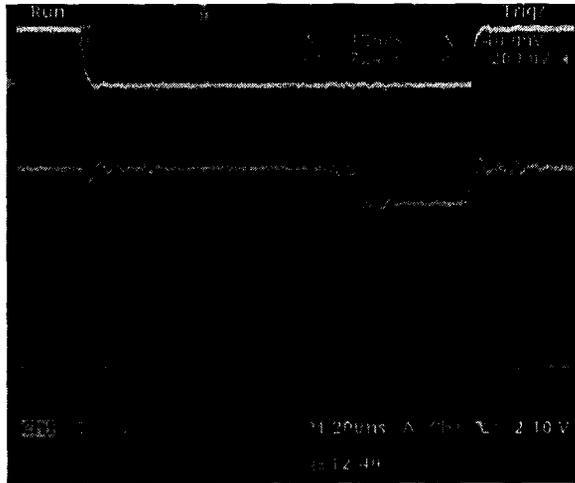


Figure 7(a). Good bit. Yellow (top trace) is Chip Enable and green (bottom trace) is bit data monitored.

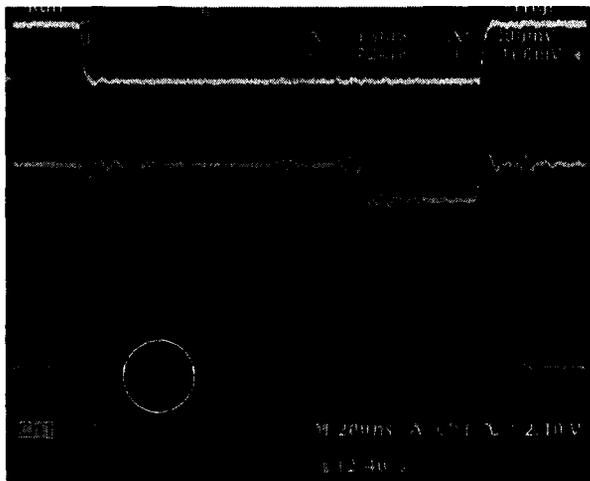


Figure 7(b). Bit beginning to fail. Note the small glitch on the bit line (cycled).

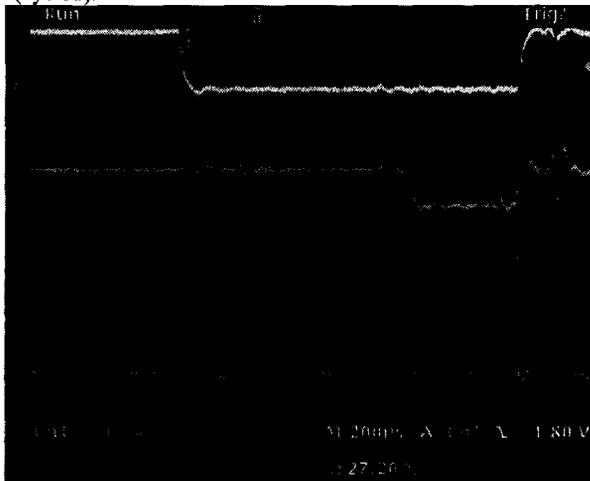


Figure 7(c). Bit eventually failed. Toggled to the correct state outside the specified timing.

#### IV. CONCLUSIONS

In this study, we have concluded that “weak cells”, due to either process-induced defective memory or poorly programmed cells, may be the root cause of the two bit failures observed on a recent NASA mission. This conclusion has not been verified by re-writing to the bad bits in flight; it is based on the statistical reliability analysis and our experimental results performed on EEPROM dice. The reliability analysis indicates that an intrinsic data retention bit failure should not be expected within the first year of operation under operating temperature of 60°C. Diagnostic and write/read cycle testing to emulate weak cells were designed and performed to demonstrate that weak cells can fail earlier than a properly programmed array and that weak cells can have low activation energy as we expected. Read cycles can accelerate data retention failures on these weak cells. We have also concluded that board timing margins need to be extensively analyzed to avoid possible program timing induced weak cells, which in turn may become early bit failures.

In conclusion, when using EEPROM in space applications, bit and page redundancy need to be included in the system architecture to enable programming around failed bit or pages. System designers must make sure that the manufacturer's specified number of write/erase cycles and specified operating temperatures are not exceeded and that the program timing meets EEPROM operation specification with necessary margin. The EEPROM should be written with all “0” and then read for a number of read cycles before burn-in testing or high temperature bake to allow the prescreen to mitigate against extrinsic escapes.

#### REFERENCES

- [1] “EEPROM Reliability Report” and “Data Retention Testing of EEPROM”, 2003, provided by the EEPROM manufacturer.
- [2] McWhorter, P. J. et al., “Retention Characteristics of SNOS Nonvolatile Devices in a Radiation Environment,” Nuclear Science, IEEE Trans. On, NS-34, Dec. 1987.

[3] Blandford, J. T. et al., "Cosmic Ray Induce Permanent Damage in MNOS EEROMs," Nuclear Science, IEEE Trans. On, NS-31, Dec. 1984.

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